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THE UNIVERSITY OF ALBERTA

CHARACTERIZATION OF CMOS MAGNETIC FIELD SENSORS

BY

Davide Romolo Briglio

A THESIS

SUBMITTED TO THE FACULTY OF GRADUATE STUDIES AND RESEARCH IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF MASTER OF SCIENCE.

DEPARTMENT OF ELECTRICAL ENGINEERING

EDMONTON, ALBERTA

SPRING 1988

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Davide Briglio

Student's signature

584, Cassiar Ave.,
Prince Rupert, B. C.,
Canada
V8J 3Z5

Date: Nov. 25 1987

THE UNIVERSITY OF ALBERTA

FACULTY OF GRADUATE STUDIES AND RESEARCH

The undersigned certify that they have read, and recommend to the Faculty of Graduate Studies and Research for acceptance, a thesis entitled Characterization of CMOS Magnetic Field Sensors, submitted by Davide Romolo Briglio, in partial fulfillment of the requirements for the degree of Master of Science.

Supervisor

Date: November 17, 1987

Beniamino ed Elisabetta Briglio

Luigi ed Innocenza Roppo

Abstract

The sensitivities of two types of CMOS magnetic field sensors are measured. The two devices are the split drain magnetic field effect transistor, MAGFET, and the vertical Hall device, VHD. For each device the influence of geometry and operating point on sensitivity is investigated and analysed. Furthermore the effects of the fabrication process are assessed by comparing identical MAGFET designs realized in two different CMOS technologies. The data from our VHDs are compared to experimental and modeling results from two other VHDs. The comparison is made in terms of the absolute sensitivity, with a constraint on the device power consumption. The MAGFET results are used to construct a low frequency small signal equivalent circuit model. In addition a method of measuring the Hall mobility and scattering factor in inversion layers is described and implemented. Extensive measurements of the low frequency output noise of various MAGFETs are also presented, which allow assessment of the sensors in terms of signal to noise ratio or resolution.

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LIST OF SYMBOLS

Symbol	Name	Unit
B	Magnetic induction vector	tesla
BW	Bandwidth	1/second
C	Capacitance	farad
C'_{ox}	Gate capacitance per unit area	farad/cm^2
d	Distance between contacts or drains	μm
E_x	Electric field in the X direction	volt/cm
E_y	Electric field in the Y direction	volt/cm
f	Force vector	newton
g_b	Magnetic transconductance	ampere/tesla
g_m	Transconductance	ampere/volt
H	Magnetic field vector	ampere/meter
I	Current	ampere
I_D	Total drain current	ampere
I_H	Hall current or current imbalance	ampere
k	Boltzmann's constant	joule/ deg. kelvin
K	Geometric factor	unitless
L	Channel or contact length	μm
L_A	Active area length	μm

n	Electron concentration	cm^{-3}
N_A	Bulk acceptor doping concentration	cm^{-3}
p	Hole concentration	cm^{-3}
P	Power	ampere-volt
q	Electronic charge	coulomb
r	Scattering factor	dimensionless
r_n	Electron scattering factor	dimensionless
r_o	Output resistance	volt/ampere
r_{DD}	Resistance between drains	volt/ampere
R_H	Hall coefficient	$cm^{-3}coulombs^{-1}$
R_C	High pass filter resistor	volt/ampere
R_L	Load resistance	volt/ampere
S_A	Absolute sensitivity	volt/tesla
S_{RI}	Sensitivity normalized to supply current	volt/ampere-tesla
S_{RV}	Sensitivity normalized to supply voltage	$tesla^{-1}$
$S_{VV}(\omega)$	Power spectral density of V(t)	watt/hertz
t	Thickness	μm
T	Temperature	degrees kelvin
v_1	Small signal voltage	volt
v_2	Small signal voltage	volt
v	Velocity vector	meter/sec
V	Voltage	volt

V_A	Early voltage	volt
V_D	Drain voltage	volt
V_{DS}	Drain to source voltage	volt
V_G	Gate voltage	volt
V_{GS}	Gate to source voltage	volt
V_H	Hall voltage or voltage imbalance	volt
V_{SB}	Source to substrate voltage	volt
V_T	Threshold voltage	volt
v_D	Small signal drain voltage	volt
W	Channel width	μm
δ	Relative current imbalance	dimensionless
ΔB	Change in magnetic induction	tesla
Δi_n^2	Noise current power	watt
$\Delta\rho$	Change in resistivity	volt-cm/amp
Δf	Frequency bandwidth	hertz
ϵ_s	Permittivity of gate oxide	farad/cm
λ	Channel length modulation parameter	1/volt
θ_H	Hall angle	degree
ρ_o	Resistivity	volt-cm/amp

ψ_B	Potential in the bulk	volt
τ	Relaxation time	second
μ	Mobility	cm^2/volt-sec
μ_n	Electron drift mobility	cm^2/volt-sec
μ_o	Magnetic permeability of free space	amp/meter-tesla
μ_p	Hole drift mobility	cm^2/volt-sec
μ_r	Relative magnetic permeability	amp/meter-tesla
μ^*	Hall mobility	cm^2/volt-sec
μ_n^*	Electron Hall mobility	cm^2/volt-sec
μ_p^*	Hole Hall mobility	cm^2/volt-sec
$\mathcal{V}(\omega)$	Fourier Transform of V(t)	volt-sec
$< >$	Averaging of quantity in brackets	

1. INTRODUCTION

The use of semiconductors in the field of electronics has produced rapid changes of technology. Semiconductor material has made possible solid state electronic devices which are smaller and more reliable than their predecessors. For electronics this has facilitated both the simplification of existing circuits and the realization of more complex circuits. The tremendous technological leap was duplicated when shortly afterwards entire circuits could be fabricated on wafers of semiconductor material. The integrated circuit produced a new age, microelectronics. The benefits of smaller size were numerous and the rush to miniaturize was on. Integrated circuits, (IC), shrunk to large scale integrated circuits, (LSI), which shrunk to very large scale integrated circuits, (VLSI). Even smaller device sizes are anticipated, and the achievement will no doubt be crowned by a larger acronym.

In this hurried change some things remained relatively unchanged, one of them being transducers. A considerable amount of electronic equipment is employed to measure physical or chemical quantities. These quantities or signals, can be grouped into six classes, electrical, magnetic, radiant, thermal, chemical and mechanical. Respective examples of each class are voltage, magnetic field, infrared radiation, temperature, ion concentration, and acceleration. Any device which converts a signal to another signal belonging to the same or a different class is considered a transducer. Transducers can be further divided into sensors and actuators.

For electrical purposes any transducer or arrangement of transducers which produces an electrical signal to serve as an input to an electrical circuit is considered a sensor, while on the other hand any transducer used to convert an electrical signal to another signal is considered an actuator. Thus for an item such as a radio the antenna serves as a sensor and the speaker as an actuator.

It is an unfortunate fact that most transducers haven't been as successfully miniaturized as present day electronics. However, a reduction in size is not the only criterion. The most desirable transducer is one that can be fabricated with minimal or no changes to present semiconductor technologies [1]. In this case the integration of a transducer and circuitry are achieved by inexpensive batch fabrication [1]. Thus, the wide gap between transducers and electronics, and the potential rewards for bridging it, is encouraging the development of novel microelectronic transducers.

Among the myriad of semiconductor microelectronic transducers there is a multitude of magnetic field sensors (MFS). Their ability to detect a magnetic field **H** is rooted in the Lorentz force, $\mathbf{f}=q\mathbf{v}\times\mathbf{B}$, where q denotes the coulomb charge, **v** the velocity and **B** the magnetic induction, with $\mathbf{B}=\mu_o\mathbf{H}$ in vacuum. The Lorentz force causes galvanomagnetic effects such as Hall voltage, carrier deflection, magneto-resistance, and magneto-concentration [1]. These effects form the basis of most semiconductor MFS.

The applications of MFS fall into two categories, direct and indirect. In direct applications the MFS serves as part of a magnetometer, used for example to measure magnetic fields or read magnetic tapes. In indirect applications the magnetic field is solely an intermediary carrier for

detecting non-magnetic signals, such as physical displacement or potential free current detection [2].

Typical semiconductor materials for MFS are Si, GaAs and InSb. A shortcoming that they share is that they are low permeability materials. The relative permeability μ_r is approximately unity. If their magnetic permeabilities were higher than unity, say as large as for ferromagnetic materials, then the resulting MFS would be extremely sensitive by virtue of $B = \mu_r \mu_0 H$, thereby magnifying the Lorentz force and any consequential galvanomagnetic effects [1]. Among each other these materials have various advantages and disadvantages. Comparatively InSb has the highest carrier mobility followed by GaAs then Si. The property of high mobility can be of advantage in device performance. Unfortunately InSb has the smallest bandgap while GaAs has the largest. This imposes temperature limitations on InSb while enabling GaAs to be used in temperatures as high as 250 ^{o}C. The chief advantage of silicon is that it is presently the least expensive material to employ [1]. Accordingly many Si magnetic field sensors have been devised.

There are presently several silicon technologies, the most prominent being Bipolar and CMOS. CMOS is the newer of the two. Due to its self isolating metal oxide field effect transistor (MOSFET), very high device densities can be reached. Each technology has advantages which make it suitable to specific circuit applications. In the way of magnetic field sensors numerous devices have been realized using either technology. The lateral magnetotransistor for instance can be fabricated in both, while the magnetic field effect transistor (MAGFET), is exclusive to MOS technology. The

magnetic field dependent phenomena occurring within these and other MFS are quite complicated and not fully understood. Hence, device design and optimization with respect to any galvanomagnetic effect is greatly aided by numerical modelling.

In this work we investigate experimentally the functioning of two magnetic field sensors, realizable in CMOS technology. The devices are, the split drain MAGFET, and the vertical Hall device, VHD. Various types of MAGFETs are dealt with, the dual drain and the triple drain variety. The dual drain group consists of a p-channel type of a single geometry, and n-channel types of differing geometries. The triple drain group consists solely of a fixed geometry n-channel type. Numerical modelling of dual and triple drain MAGFETs indicate that the latter has a higher sensitivity than the former, at least in the MOS linear region of operation [2]. One objective was to verify this result and to determine if it remains true even in the saturation region. The VHD was fabricated only in n-substrate, and not in p-well.

The objective of this work goes beyond the tabulation of device performance. The characterization of these devices serves many other purposes. The results can serve as a guide or check for numerical modelling programs. Owing to the complexity of the galvanomagnetic phenomena occurring within various devices, their operation is understood mostly qualitatively or even speculatively. Provided that a numerical model predicts, or can be adjusted to predict, fairly accurately the output characteristics of a device, then more faith can be placed on its predictions as to what occurs within the device. In turn this provides information as to which, or to what degree, galvanomagnetic effects occur.

Ultimately these sensors can be integrated with signal processing

circuitry on the same chip. Most electronic circuits are now designed with the aid of a computer circuit simulation program such as SPICE. The construction of an equivalent circuit model of a sensor is then an asset. The design process is eased since the circuitry and sensor can be computer simulated together.

Aside from providing response curves, extensive testing can uncover various subtle or complicated phenomena occurring within devices. Sensitivity can be investigated as a function of biasing point. This can lead to optimization of device performance, and insight as to what is happening within the device itself. Device noise is as crucial as sensitivity in terms of overall performance. Furthermore, noise measurements can be indicative of fundamental microscopic behaviour. Once the device properties of sensitivity and noise are known then optimal modes of operation can be identified and the device can be better matched to its scope of applications.

It is also essential to know the device tolerance to the fabrication process, and conversely the suitability of a process to a particular sensor design. Immunity of the terminal characteristics to the process makes the sensor more practical and easier to integrate. On the other hand these magnetic sensors can become a means of establishing a process parameter to aid in evaluating or comparing processes.

The contents of the following sections are now outlined. The next chapter serves to acquaint the reader with the magnetic field sensors tested. A brief account is given of how magnetic field and current interact to enable the electronic detection of magnetic field. The operation of the MAGFET and VHD is then described, together with numerical modelling results of current and equipotential distributions within these devices.

Chapter three deals with the experimental procedure. A description is given of the equipment used and how it is configured. The devices tested are then more thoroughly described. Finally, the steps involved in the various tests are explained.

The predominance of device characteristics and sensitivity are contained in chapters four and five. In chapter four the results from the various MAGFET geometries are presented and discussed. Most of the results demonstrate how sensitivity varies with biasing. The remaining results show some important zero field D.C. characteristics. Combining measurement and modelling results, a means of deriving inversion layer Hall mobility is demonstrated. As well, two 5 μm processes are compared, Microtel Pacific ISO-CMOS and Northern Telecom CMOS1B. Chapter five deals with the VHD in a similar fashion. Included here is a sensitivity comparison of our VHDs with a VHD designed and tested by Popovic [3], and a VHD numerically modelled by Huiser and Baltes [4].

In chapter six a low frequency circuit model of the dual drain MAGFET is developed. Results from using the square MAGFET as a combined sensor and amplifier are presented. The device response to magnetic field is compared to what is predicted by the developed circuit model.

The results from noise measurements on the dual drain MAGFETs are presented in chapter seven. The spectra are for noise voltage originating from a single drain, between drains, and for the MAGFET operating as a MOSFET. Signal to noise ratios and the influence of magnetic field on device noise levels are presented.

In chapter eight the conclusions are given. The major findings and

implications of the sensitivity and noise measurements are summarized. Additional comments, speculations and viewpoints are expressed.

In Appendix A estimates of the measurement errors in the experiments conducted are presented. Appendix B deals with the sensitivity in terms of relative current imbalance, and the effect of the averaging procedure used. Appendix C contains output characteristics of the Northern Telecom dual drain MAGFETs.

2. PREVIOUS WORK

2.1 Magnetic Field Detection

To familiarize ourselves with galvanomagnetic effects occurring within semiconductors we start with the expression for the Lorentz force;

$$\mathbf{f} = q\mathbf{v}\times\mathbf{B}\,. \tag{2.1}$$

This equation implies that a particle of charge q with velocity v exposed to a magnetic field B will experience a force f perpendicular to both the velocity and magnetic field vectors. This effect coupled with such factors as type of carrier, material band structure, and sample geometry can produce a variety of galvanomagnetic effects which can ultimately be used to detect magnetic fields.

For purposes of illustration consider a unipolar isothermal rectangular semiconductor sample of length L width W and thickness t, lying in the X-Y plane as shown in Fig. 2.1. With current flow along the X direction and a perpendicular magnetic field in the Z direction, current carriers will be deflected in the negative Y direction. This creates an electric field in the Y direction which opposes the Lorentz force on the carriers. The electric field in the Y direction will produce a voltage across the width of the sample known as the Hall voltage. The Hall voltage near the centre of a long thin plate, (L>>W>>t), is given by [5];

$$V_H = R_H IB/t\,, \tag{2.2}$$

$$R_H = 1/nq \,. \qquad (2.3)$$

R_H is called the Hall constant and n represents the carrier concentration. The sign of the resulting Hall voltage indicates the sign of the current carriers. The angle between the current density and resultant electric field lines is called the Hall angle, and is given by[5];

$$\tan \theta_H = E_y / E_x = \mu B \,. \qquad (2.4)$$

In Fig. 2.2 the current and equipotential lines inside two finite sized Hall plates are shown. They are the outcome of numerical modelling using a finite difference scheme [6]. Since equipotential lines are orthogonal to the electric field lines the angle between intersecting current and equipotential lines is $\theta_H \pm 90°$. The long thin Hall plate is part (a) of Fig. 2.2.

For a semiconductor with spherical constant energy surfaces, with both positive and negative carriers contributing to conduction, and relaxation times for holes and electrons that vary in the same way with energy, the expression for Hall voltage is identical to equation (2.2). Provided again that L>>W>>t, the Hall constant is now given by [5];

$$R_H = -r\,(p\mu_p^2 - n\mu_n^2)/\, q(p\mu_p + n\mu_n)^2 \,, \qquad (2.5)$$

$$r = \langle \tau^2 \rangle / \langle \tau \rangle^2 \,. \qquad (2.6)$$

The hole and electron concentrations are represented by p and n, and their corresponding drift mobility by μ_p and μ_n. The factor r is the ratio of the average of the relaxation time squared to the square of the average relaxation time. This accounts for scattering mechanisms, and the fact that not all carriers have the same velocity. The terms of the form < > imply averaging of the quantity contained within the brackets. The average is over energy with an appropriate weighting function [5]. Moreover, this introduces the following change to equation (2.4) [5];

$$\tan \theta_H = r\mu B = \mu^* B. \qquad (2.7)$$

From the earlier unipolar example it can be deduced that whether the current carriers are holes or electrons they are both deflected to the same side. Thus, for bipolar conduction the Hall voltage is reduced, as indicated by equation 2.5. Under the condition that $p\mu_p^2 = n\mu_n^2$ we get $R_H = 0$, and no Hall voltage will result.

If in the unipolar rectangular sample an electric field is applied in the Y direction to cause current flowing across the width of the sample the phenomenon of carrier deflection can be demonstrated. In this configuration the Hall field developed across the length of the sample is negligible compared to the applied field and the Lorentz force is essentially unopposed. Again, everywhere in the sample the Hall angle between current and electric field lines must be given by equation (2.7). This fact is

accommodated by the carriers being deflected an angle θ_H from the applied electric field. The situation using current and equipotential lines is depicted in Fig. 2.2 (b).

These two manners of using a rectangular sample are related through the Van Der Pauw duality theorem [7]. Provided the material is a solid of cubic crystal symmetry both rectangular samples yield the same information, as for example Hall mobility. However it has been pointed out that for non cubic solids these two configurations can produce different Hall mobilities [8]. In figure 2.3 (a) we have a rectangular sample configured to measure Hall voltage. The accompanying sample in part (b) can be created by removing the electrical contacts of (a) and making contacts to regions where there are no contacts in (a). The configuration of Fig. 2.3 (b) is suitable for measuring current imbalance between contacts on the same side of the sample. For a wide thin plate, (W>>L>>t), the current imbalance $(I_1-I_2)=I_H$, is given by [8];

$$I_H = (L/W)I\mu^* B . \qquad (2.8)$$

If the semiconductor material is anisotropic then effects such as transverse and longitudinal magneto-resistance can occur. This provides another means of detecting magnetic fields. However, even if the material is isotropic transverse magneto-resistance can occur. This is possible under the conditions that the carriers have an energy independent relaxation time, and that both carrier types present [5]. For one carrier type with an energy dependent relaxation time the change in resistivity $\Delta\rho$ from its zero field

value ρ_o is [5];

$$\Delta\rho/\rho_o = (\mu^* B)^2(\langle\tau^3\rangle\langle\tau\rangle/\langle\tau^2\rangle^2 - 1). \qquad (2.9)$$

The relaxation time is denoted by τ. In equation (2.9) the right most portion bounded by the ( ) parentheses is approximately 0.28 for lattice scattering [5]. Thus for $\mu^* B<1$ the transverse magneto-resistance effect can be very small.

2.2 The MAGFET

The first magnetic field effect transistor (MAGFET) was devised by Gallagher and Corak [9]. The inversion layer of a MOSFET served as a Hall plate. The Hall voltage was detected by diffusing Hall contacts on the sides of the channel. Using a similar MOS structure with multiple Hall contacts Fry and Hoey discovered that current imbalance could be used to detect magnetic field [10]. The split drains in their MAGFET where actually Hall voltage contacts. Since current is constrained to flow along the chip surface the MAGFET is essentially sensitive to magnetic fields perpendicular to the chip surface.

The split drain MAGFETs designed for this work are true to their name, (Fig. 2.4). The drain diffusion is not continuous across the channel width, but comprised of two or three distinct diffusions. Considering the dual drain MAGFET in terms of geometry, it possesses symmetry about a bisecting line from source to drain. At zero field, because of this symmetry, the drain current lines run straight and parallel form source to drain, except near the

vicinity of the drain separation. Accordingly the two drain currents should be equal. The application of a magnetic field perpendicular to the channel disrupts the symmetry of the current lines causing a current imbalance at the drains. This device is reminiscent of a Hall plate's Van Der Pauw dual. The current and equipotential lines with an applied magnetic field for the dual and triple drain MAGFETs are shown in Figs. 2.5 and 2.6 respectively. They were generated by numerical modelling [11, 12].

2.3 The Vertical Hall Device

The Vertical Hall Device (VHD) was invented by Popovic as a means of using the Hall effect to detect magnetic fields parallel to the chip surface [3]. The geometry and name of the device arose form the idea of imbedding a Hall plate vertically into the chip surface and conformally deforming the sides so that they come to rest on the chip surface, (Fig. 2.7).

Under zero field conditions, if the device is operated in the proper fashion electrically, the current and voltage lines within the device possess a degree of symmetry. To achieve this the centre terminal can be connected to a current or voltage source with the two outer terminals grounded. The two remaining inner terminals can be used as Hall voltage probes. Half of the total device current will then flow through each outer terminal, while the voltage at the two inner terminals will ideally be the same. An applied magnetic field disrupts this symmetry, facilitating the simultaneous detection of the field with current or voltage imbalance. This situation is demonstrated if Fig. 2.8, which is also a product of numerical modelling [4].

2.4 Device Sensitivity

To rate the performance of a magnetic sensor there are several definitions of sensitivity to choose from [1]. Consider the VHD if Hall voltage is used as the measure of magnetic field strength. Sensitivity can be defined as;

$$S_A = |\partial V_H/\partial B|_{I=const} \quad [V/T]. \tag{2.10}$$

This is an absolute sensitivity, with **B** perpendicular to the plane shown in Fig. 2.7 (b). It is also possible to define sensitivities relative to supply current or voltage;

$$S_{RI} = |I^{-1}\partial V_H/\partial B| \quad [V/AT], \tag{2.11}$$

$$S_{RV} = |V^{-1}\partial V_H/\partial B| \quad [1/T]. \tag{2.12}$$

For the VHD, the results will be reported in terms of equations (2.10) to (2.12), as well as (2.13) below.

If current imbalance is the measure of magnetic field then a suitable definition is;

$$S_R = |I^{-1}\partial(I_1-I_2)/\partial B|_{B=0} \quad [1/T]. \tag{2.13}$$

This is applicable to both the MAGFET and the VHD, with **B** being

perpendicular to the planes shown if Figs. 2.4 and 2.7 (b). The quantity I is the sum of the currents I_1 and I_2. Most of the test results with respect to bias point are plotted with the relative current imbalance as the ordinate;

$$\delta(B) = |(I_1(B)-I_2(B))/(I_1(B)+I_2(B))| . \qquad (2.14)$$

In this definition the current imbalance at a particular field is referenced to the sum of the terminal currents at the same field rather than at zero field. Furthermore the equation is meaningful for terminal currents being equal at zero magnetic field. The devices tested all suffer some degree of current offset. This offset can be virtually eliminated by taking the average of equation (2.14) at identical magnitudes of positive and negative field strength. The procedure is valid provided that the response to magnetic field is linear, and that the total current changes very little with magnetic field, (see Appendix B). In the results the relative current imbalance is generally expressed as a percentage.

2.5 Carrier Mobilities

Mobility is a measure of how easily current carriers can move through a medium. With the flow of current in the presence of a magnetic field there are two mobilities to contend with, drift mobility which pertains to the applied electric field, and Hall mobility which pertains to the influence of the magnetic field. Hall and drift mobilities are related by the expression [5];

$$\mu^* = r\mu . \qquad (2.15)$$

Where as usual μ represents the drift mobility, μ^* the Hall mobility and r the scattering factor. The value of r is determined by energy band structure and scattering mechanisms. In bulk silicon a measured value of the electron scattering factor is $r_n = 1.15$, for low donor concentration at room temperature [13]. Theoretical values for impurity and phonon scattering are respectively, $r_n = 1.93$, and $r_n = 1.18$ [14].

In silicon inversion layer there is the additional mechanism of surface scattering at the Si/SiO_2 interface. In 1968 Coleman, Bate and Mize [15] using a p-channel Hall MAGFET obtained a hole scattering factor of $r_p = 0.8 \pm .03$, close to Zemel's [16] theoretical value of .88. Their results also showed that the hole Hall mobility depends on crystal orientation, mechanical stress and operating condition such as $(V_G - V_T)$. Other investigations have produced hole scattering factor values of $r_p = .92$ [7], and $r_p = .6$ [17].

Numerous experimental investigations of carrier transport in silicon inversion layer using the MOS structure have been conducted, [15, 18, 19, 20, 21]. The general result is that the Hall and drift mobility of holes and electrons exhibit a peak with respect to gate voltage. Even under a variety of substrate dopings, positive fixed oxide charge concentrations, crystal orientations and temperatures the peaking persists. Decreasing the temperature increases the magnitude of the peak while making it more prominent. For the purposes of MOS device modelling Sun and Plummer [20] measured the value of the peak drift mobility as a function of substrate doping and fixed oxide charge concentration. They found that the peak drops

as any of these quantities are increased. Fang and Fowler [18], using a circular coaxial FET observed a double peak in electron drift mobility at temperatures around 100 ^{o}K. Coleman et al. [15] reported only a single peak in the Hall mobility at 77 ^{o}K, using a rectangular MOSFET with lateral Hall contacts. The previously mentioned papers studied transport phenomena in Si inversion layers using a MOS device of fixed geometry. Throughout the literature this seems to be the case. There appears to be no study done on how the peaking in Hall or drift mobility is affected by device geometry.

Stern and Howard [22] have developed a theory which can account for the peaking in mobility with respect to gate voltage. Their analysis was concerned with the effect of Coulomb scattering on electrons in inversion layer. At low temperatures when phonon scattering is negligible, the dominant mechanisms are Coulomb and surface roughness scattering. Furthermore at low gate voltages when the surface electric field normal to the channel is small, Coulomb scattering is of more relative importance than surface roughness scattering. Coulomb scattering centres consist of fixed oxide charges, interface state charges and ionized impurities [20]. Electrons in the inversion layer effectively screen the potential due to such charges, in turn reducing their scattering ability. As the electron density in the inversion layer increases so does the amount of screening. Higher carrier density in the inversion layer is achieved with higher induced gate fields, i.e. higher gate voltages. The overall effect of screening is mobility increasing with gate voltage. However as the gate induced field increases surface scattering begins to dominate, which reduces mobility. Thus the screening of Coulomb scattering centres coupled with a mobility reducing mechanism can be seen to produce a maximum in mobility.

This Coulomb screening theory has been compared to experimentally derived drift moblities [22, 23]. Cheng and Sullivan [23] find that in their experiments the screening effect is not totally satisfactory, and that other scattering mechanisms have to be accounted for at low temperature and gate field.

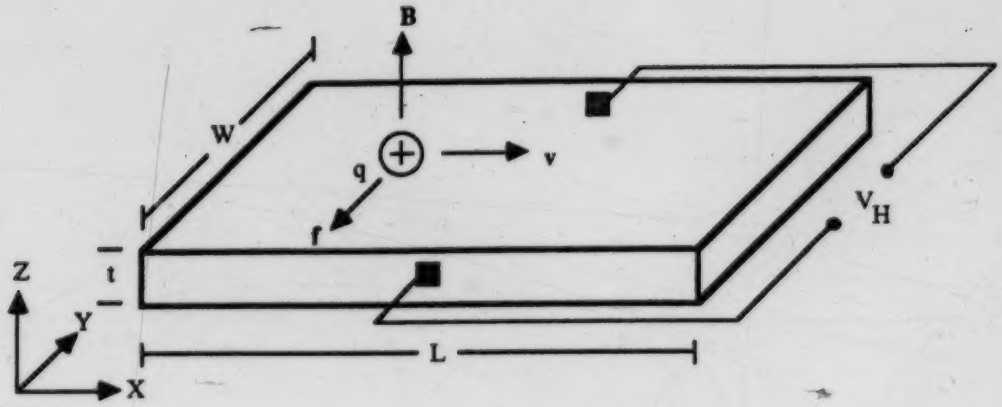

Fig. 2.1 Hall voltage and Lorentz force in a rectangular semiconductor sample.

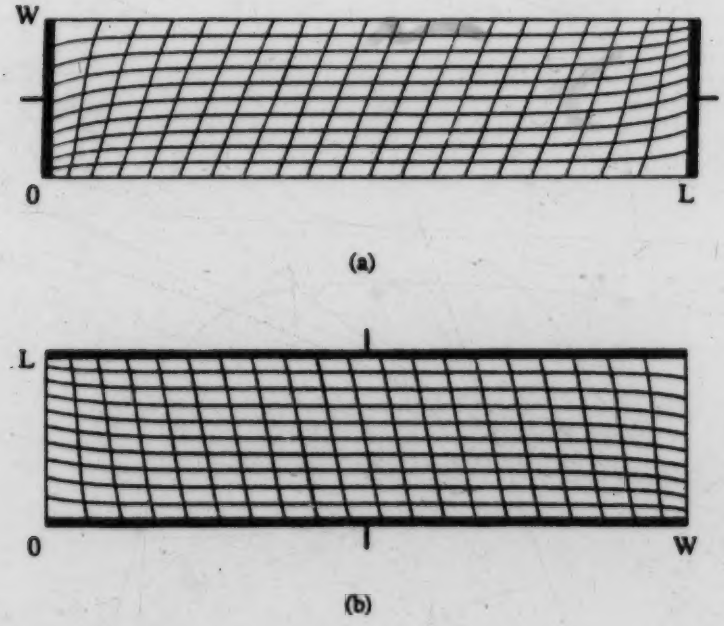

Fig. 2.2 A top view of current and equipotential lines in a long Hall plate (a), and a wide Hall plate (b).

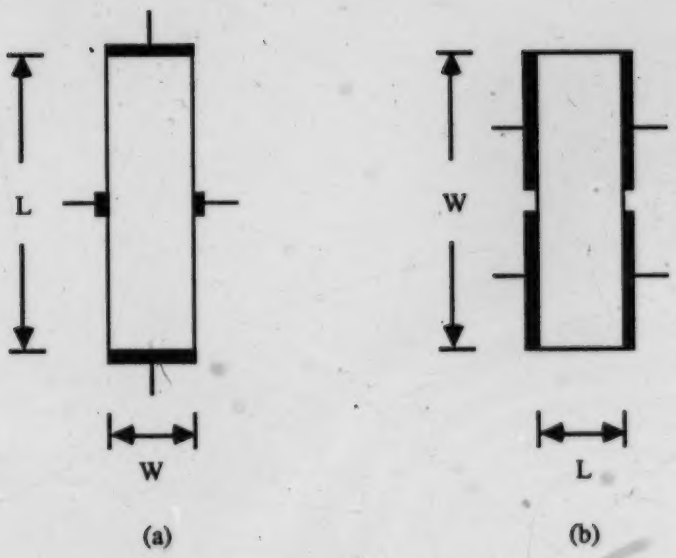

Fig. 2.3 A sample for Hall voltage measurement (a), and its Van Der Pauw dual (b).

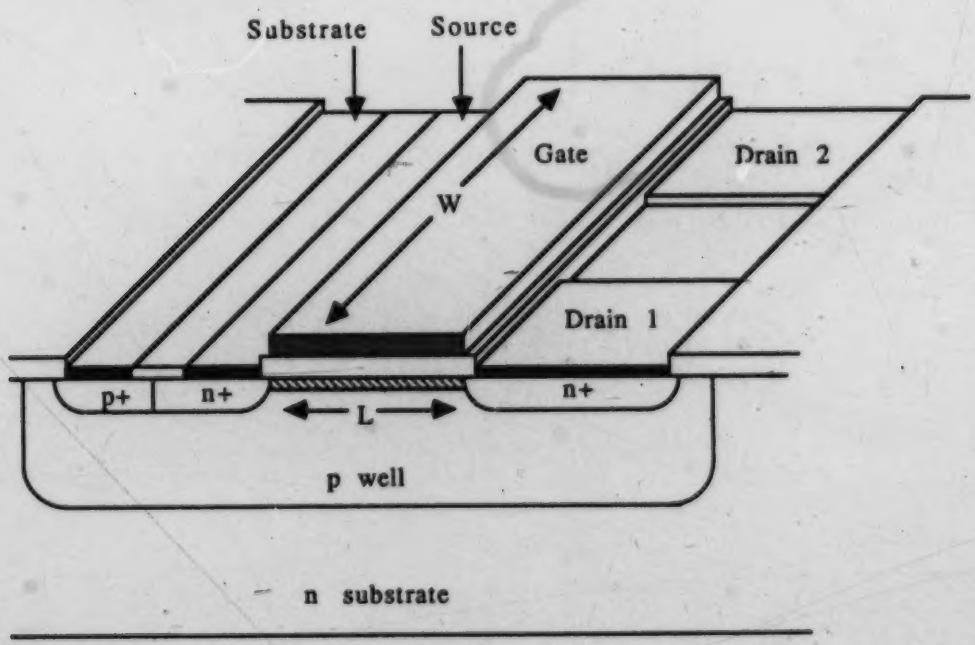

Fig. 2.4 The dual drain MAGFET structure.

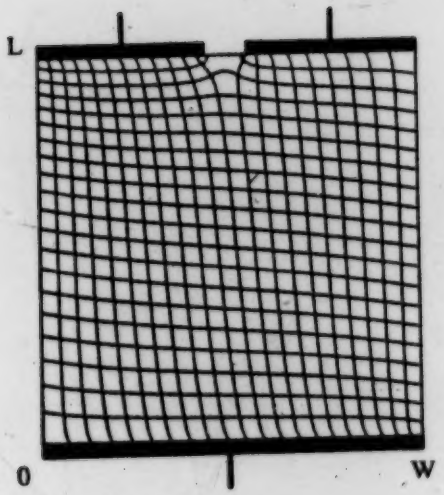

Fig. 2.5 A top view of current and equipotential lines in a dual drain MAGFET.

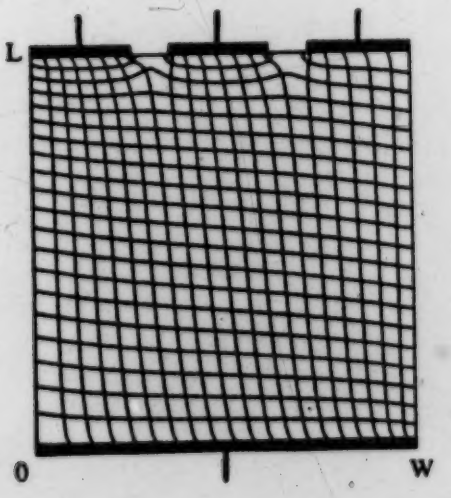

Fig. 2.6 A top view of current and equipotential lines in a triple drain MAGFET.

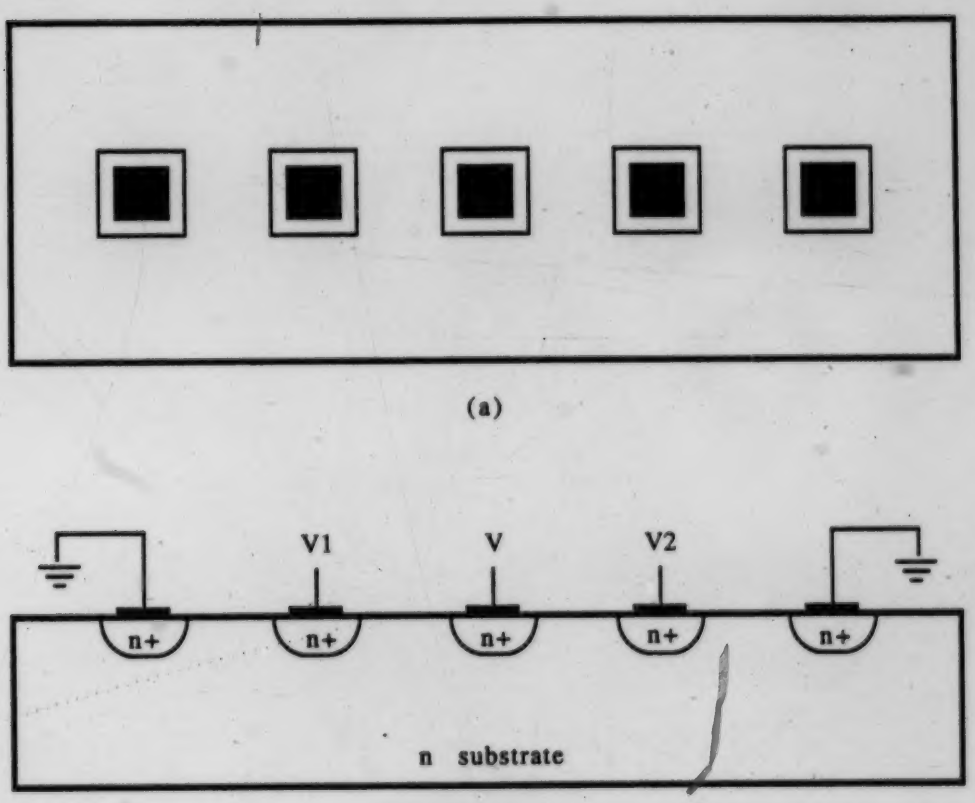

Fig. 2.7 The Vertical Hall device (VHD) structure, top view (a), and sectional view (b).

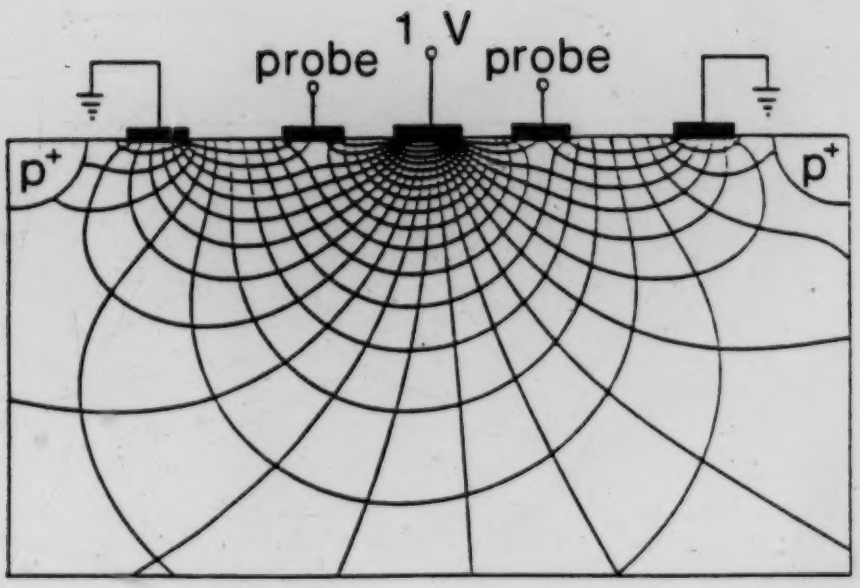

Fig. 2.8 Current and equipotential lines in the VHD.

3. EXPERIMENTAL PROCEDURE

3.1 Test Equipment Setup

The experimental setup for determining device response to magnetic field is shown symbolically in Fig. 3.1. The magnetic field is generated by a Varian V-4005 four inch electromagnet, driven by a Varian V-2900 regulated magnet power supply. Fields of up to 1.5 T can be created. The magnetic field is monitored by an LDJ-511 gaussmeter using an axial InSb Hall probe. The probe and meter have an accuracy of 1% each. From 0.2 Tesla and beyond the magnitudes of the probe's response when aligned parallel and antiparallel to the field are unequal. To compromise an average of the two readings is used and the probe error is increased to 2%. The arrangement can determine the magnetic field to an accuracy of about ±3%. The HP-4145A semiconductor parameter analyser provides the biasing points for the devices under test. Voltages can be set to an accuracy of approximately .15%, with a resolution of 1.0 mV. Voltages are measured to the same accuracy with a resolution of .05%, to at most 1.0 mV. Currents can be set or measured to a typical accuracy of .5%. The setting resolution is .1% to a maximum of 1 pA. The resolution of current measurement is also .1%, but to a maximum of 50 pA. A more extensive measurement error analysis can be found in Appendix A. Raw data provided by the analyser are stored and processed with the HP-216 personal computer. The computer is also capable of operating the analyser, facilitating the thorough testing of numerous samples.

3.2 The Samples

To observe relationships between geometry and sensitivity, six different MAGFETs were designed and fabricated, see Fig. 3.2. Five of the devices are n-channel and the sixth p-channel. The preference for n-channel devices is due to electrons having a higher mobility than holes. Two of the n-channel dual drain MAGFETs have aspect ratios, (Channel width/Channel length), of 4:1 and 1:4 to approach the limiting geometries of very wide (W>>L), and very long (L>>W) channels. Another two dual drain MAGFETs have identical aspect ratios of 1:1, but differ in size, 100 μm and 25 μm square, to investigate any effects of scaling. The fifth n-channel device is a triple drain MAGFET. The drains for this device are all of the same width. The separation between drains is 20 μm. To observe the relative performance of p and n type devices a dual drain PMOS MAGFET was designed with an aspect ratio of 3:1. Drain separation in all of these devices is 20% of the overall width. The separation always involved the breaking of various design rules, which are of course suited to producing conventional MOS transistors. Such design rule errors were disregarded since they were judged to have no bearing on the integrity of the MAGFET structure.

All of these MAGFETs were fabricated in two CMOS technologies, Microtel Pacific ISO-CMOS and Northern Telecom CMOS1B, both of which are 5 micron processes. Surface characteristics such as carrier mobility are affected by the process and it is quite unlikely that two different processes can produce exactly the same characteristics. Even two adjacent transistors on the same chip can show different characteristics. Since MAGFETs are surface devices the influence of the process on sensitivity can be investigated giving an

indication of the relative merits of the Microtel and Northern Telecom technologies.

To investigate the behaviour of the vertical Hall device two geometries were realized in the CMOS1B process, (see Fig. 3.3). In each case the contact width and the spacing between contacts are identical, W=10 μm and d=30 μm. The difference is in the length of the contacts. Short contacts, L=10 μm, to approximate ideal point contacts and long contacts, L=150 μm, to approach the other extreme. For both VHDs the contacts are centred in the device active area, such that the smallest distance from a contact to the edge of the active area is 30 μm. In the MOS process the active area is the area on the chip surface not covered by the thick field oxide layer. The respective widths and lengths of these areas are, W_A=230 μm, L_A=240 μm for the long VHD, and W_A=230 μm, L_A= 70 μm for the short VHD.

Since the VHD is sensitive to fields parallel to the chip surface it was not packaged in a standard dual in line pin package (DIP). In a DIP package the chip rests in a depression, the sides of which are partly covered in ferromagnetic material. This was anticipated to cause magnetic shielding. Therefore the VHD chips are mounted on a copper plug and plate and attached to a printed circuit board. The chip, copper plug and plate are bonded to one another with thermally conductive silver epoxy to ensure adequate heat dissipation.

3.3 Current Imbalance Procedure

The tests performed demonstrate the device response to fields varying

from -1 T to +1 T for a few biasing points, and the dependence of response on the biasing point for a constant field of one tesla. The devices are placed in a uniform D.C. field, monitored by the gaussmeter. The analyser establishes the necessary voltages and currents and measures the resulting currents and voltages, (See Fig. 3.4 for the MAGFET.). Depending on the device and its mode of operation the response can be expressed in terms of Hall voltage or current imbalance. The relative imbalance between two terminal currents is calculated using equation (2.14).

The availability of variable or constant voltage sources from the H.P. analyser is well suited to testing the dual drain MAGFETs over a wide range of bias points for a constant magnetic field. For instance two variable voltage sources, independent and equal, can be produced to power the drains, while a separate variable voltage source can be created to operate the gate. This arrangement facilitates the determination of the individual drain currents and the elimination of offsets. In the case of the triple drain MAGFET three equal and independent variable voltage sources are not available. This problem is circumvented by performing the measurement at a given field twice. With the two equal and independent voltage sources available, the middle drain is connected to drain one for the first measurement run, and then to drain two for the second run. From the four current levels measured the individual drain currents can be calculated.

For testing the magnetic field sensitivity of the VHD the centre contact is connected to a current source while the outside contacts are grounded, (See Fig. 3.5). The two remaining contacts are used as Hall voltage probes. This mode of operation is similar to that used by other investigators, [3, 4]. During

any measurement the gate is connected to ground, since for $V_G \geq 1$ the device is inoperable. To cover a large range of operating conditions the VHDs are tested at current levels that escalate by factors of ten. The point contact VHD is tested at 10 μA, 0.1 mA, and 1.0 mA, resulting in voltage levels from approximately 20 mV to 2.0 V at the centre contact. The long VHD, because of its lower resistance between contacts, is tested at current levels of 0.1 mA, 1.0 mA, and 10.0 mA. This produces voltage levels of about 35 mV to 4.0 V at the centre terminal.

3.4 Mobility Determination

In the case of the Hall MAGFET operating in the MOS linear region the resulting Hall voltage is approximately given by [1];

$$V_H = G(W/L)\mu^* B V_{DS}. \tag{3.1}$$

Where W and L denote the channel width and length respectively. The applied drain to source voltage is represented by V_{DS}. The MOS linear region is obtained under the conditions $|V_{GS}| > |V_T|$, and $|V_{GS} - V_T| > |V_{DS}|$. The quantity V_T is called the threshold voltage, representing the voltage level that the gate to source voltage must overcome in order to produce an inversion layer at the surface. The factor G is dimensionless and accounts for the specific MAGFET geometry, (W, L, position and size of the Hall contacts), with G=1 in the limit L>>W.

In the split drain MAGFET the Lorentz force produces an imbalance between the two drain currents. The relative current imbalance can be used as a measure of the magnetic field or as a means of determining Hall mobility.

For sufficiently small B and drain voltage $V_{D1} = V_{D2}$ the relative current imbalance is approximated by [24];

$$I_H = K \mu^* B I . \qquad (3.2)$$

The dimensionless factor K accounts for the specific geometry, (W, L, and drain separation), with K=L/W for W>>L, W>>d. For arbitrary geometries the factor K can be determined by numerical modelling. Using relation (3.2) and the computed values of K with experimentally measured relative current imbalance at a known magnetic field strength permits the calculation of Hall mobility in inversion layers. The choice of the voltage on the two drains is 0.1 V. The magnetic field levels used are +1 T and -1 T. Again, the relative imbalance is calculated using equation (2.14).

Operating the MAGFET as a regular MOS transistor it is possible to ascertain the drift mobility with the following equation [14];

$$I_D = \mu C'_{ox}(W/L)((V_G - V_T) - (1/2 + (\epsilon_s q N_A / |\psi_B|)^{1/2} / 4C'_{ox}) V_D) V_D \qquad (3.3)$$

Here ϵ_s denotes the permittivity of the gate oxide, C'_{ox} the gate oxide capacitance per unit area, V_T the threshold voltage, N_A the doping concentration, and ψ_B the potential in the bulk. Equation (3.3) is an approximation for the drain current in the MOS linear region of operation under the conditions $V_D < (V_G - V_T)$, and $V_D < 2\psi_B$ [14, 25]. The drift mobility is

calculated by measuring I_D at V_D=0.0 and V_D=0.1 V, then equating $\Delta I_D/\Delta V_D$ to $\partial I_D/\partial V_D$ of equation (3.3). The term $(1/2+(\varepsilon_s q N_A/|\psi_B|)^{1/2}/4C'_{ox}) \approx .9$ becomes negligible as (V_G-V_T) exceeds one volt, or V_G>2.0 V. With a knowledge of the Hall and drift mobility the scattering factor in the inversion layer can be obtained from the relation $r = \mu^*/\mu$.

The n-channel Northern Telecom dual drain MAGFETs tested are the 100 μm x 100 μm, 100 μm x 25 μm, and 25 μm x 100 μm. The range of gate voltage for the drift and Hall mobility measurements is 0.6 to 5.6 V, in 0.2 V increments. The values of $N_A=1x10^{16}$ (cm^{-3}) and C'_{ox}=40.6 (nF/cm^2) are obtained from the SPICE and electrical parameters documented by the Canadian Microelectronic Corporation (CMC) [26]. These values serve as a guide for analog circuit design and do not appear with any standard deviation.

3.5 Noise Measurement Procedure

The noise measurements are performed with the batteries, device under test, and the amplifier shielded by a 0.375 inch steel container, (see Fig. 3.6). The batteries are of the rechargeable sealed lead acid type. To reduce coupling between the device under test and the amplifier, each has a separate power supply. The amplifier output is connected to a digital signal analyser, which employs a Fast Fourier Transform (FFT) algorithm to calculate the signal spectrum.

The specific signal analyser used is an H.P. 3561A. It has a frequency range of D.C. to 100 kHz. However, for sake of measurement time, amplifier bandwidth and input requirements, the spectra are measured from 0.1 Hz to

100 kHz, or 1.0 Hz to 100 kHz. The analyser frequency resolution is proportional to the frequency span of the measurement. To ensure relatively narrow band measurements the entire span is constructed from measurements on smaller frequency spans, (see Table 3.1). To smooth any measured spectra the analyser's root mean square (RMS) averaging algorithm can be employed. The first step of the process is the Fourier Transformation (FT) of a discretely sampled time signal V(t);

$$\mathcal{V}(\omega) = FT\{V(t)\} . \tag{3.4}$$

The amplitude of $\mathcal{V}(\omega)$ at each frequency point is squared. Since $\mathcal{V}(\omega)$ is in general complex this is equivalent to the product of $\mathcal{V}(\omega)$ with its complex conjugate $\mathcal{V}^*(\omega)$;

$$|\mathcal{V}(\omega)|^2 = \mathcal{V}(\omega)\mathcal{V}^*(\omega) . \tag{3.5}$$

The next step is the averaging of (3.5) over m, the number of transformed time signals. Division by the measurement bandwidth (BW) results in the power spectral density (PSD), $S_{VV}(\omega)$ of V(t):

$$S_{VV}(\omega) = \langle \mathcal{V}(\omega)\mathcal{V}(\omega) \rangle = (1/mBW) \sum_{i=1}^{m} \mathcal{V}_i(\omega)\mathcal{V}_i^*(\omega) . \tag{3.6}$$

The number of averaged readings for each frequency span is shown in Table

3.1. All of the spectra recorded are noise voltage power spectral densities $S_{VV}(\omega)$, in units of decibels per hertz (dB/Hz). A sinusoidal input signal of 1 V zero to peak produces a reading of -3 dB/Hz. Converted back to a RMS voltage this figure gives $(1/\sqrt{2})$ V/Hz, which is the known RMS factor for sinusoidal voltages.

To measure spectra from a single drain a Brookdeal 5004 single input amplifier is used. It has a bandwidth of 0.5 Hz to 1.0 MHz. For noise spectra from between two drains a Brookdeal 5006 differential amplifier is used. It has a bandwith of 0.1 Hz to 1.0 MHz. Both amplifiers are stipulated to have a fixed gain of 60 db ± .3 dB. This is not valid over the specified bandwidth, since the bandwidth is computed from the -3 dB frequency points. To compensate for any variation, the amplifier gain is measured from .1 Hz to 100 kHz. The results from the gain versus frequency measurements are used to adjust the appropriate spectrum.

The device and its biasing circuitry is shown in Fig. 3.7. The load resistors R_{L1}, R_{L2} and the high pass filter resistors R_{C1}, R_{C2} are all of the low noise metal film type. As well, for sake of low noise C_1 and C_2 are metalized polyester film capacitors. For purposes of keeping the drains similarly loaded the two high pass filters are connected to their respective drains whether a differential or a single drain noise measurement is performed.

The 100 µm square MAGFET is the only device tested in the MOS linear region. In this case the operating voltages are V_{GS}= 6.3 V, V_{DS}= 0.9 V and V_{DD}= 6.3 V. Three NMOS MAGFETs are tested in the saturation region, the 100 µm x

100 μm, the 100 μm x 25 μm, and the 25 μm x 100 μm. The typical operating voltages for each device are V_{GS}= 6.3 V, V_{DS}= 8.5 V, and V_{DD}= 12.7 V. The drain load resistance values for the various noise measurements are shown in table 3.2. The individual drain load resistances are equal to the extent that the resistors are the same standard value. No effort is made to trim the load resistance value to obtain similar drain bias voltages. For noise measurements made with the drains shorted to one another the same load resistors remain in the circuit. The drain noise voltage of each MAGFET with ~~one~~ drain operating is also measured. In this test one drain is left floating while the active drain is loaded with a resistor. The resistor value chosen is that which would give approximately the same drain voltage as when both drains are operating.

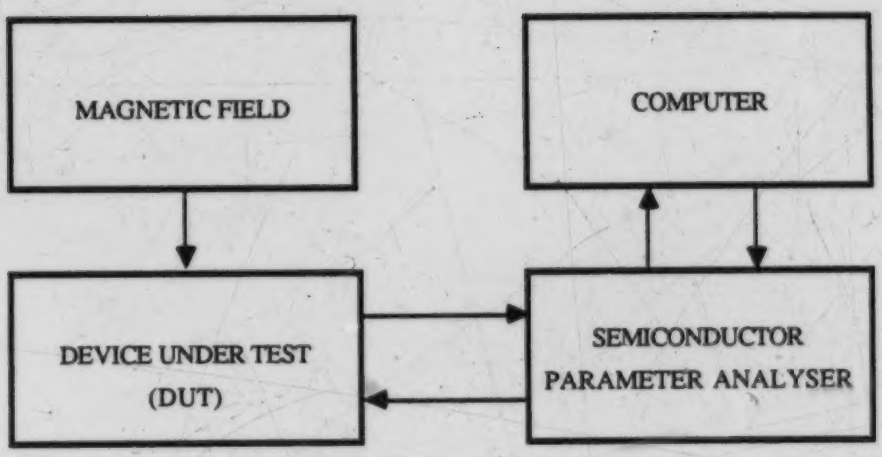

Fig. 3.1 Experimental setup to measure current imbalance.

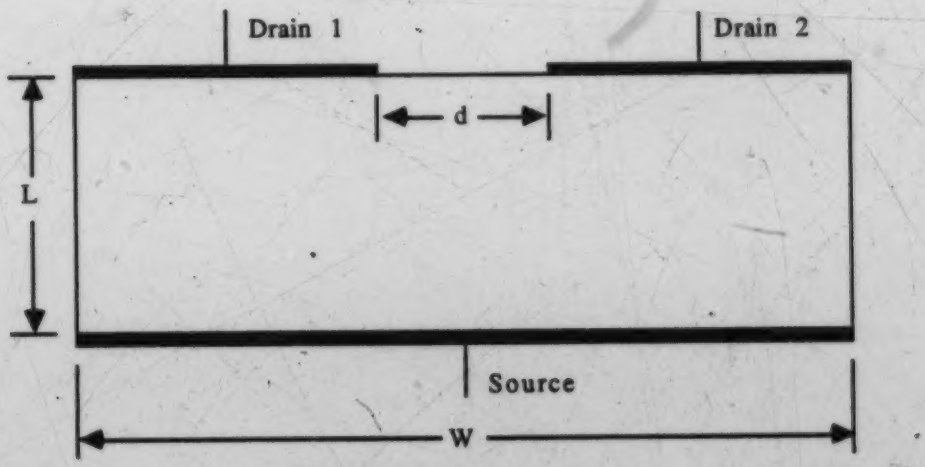

Fig. 3.2 Dimensions of the MAGFET geometry.

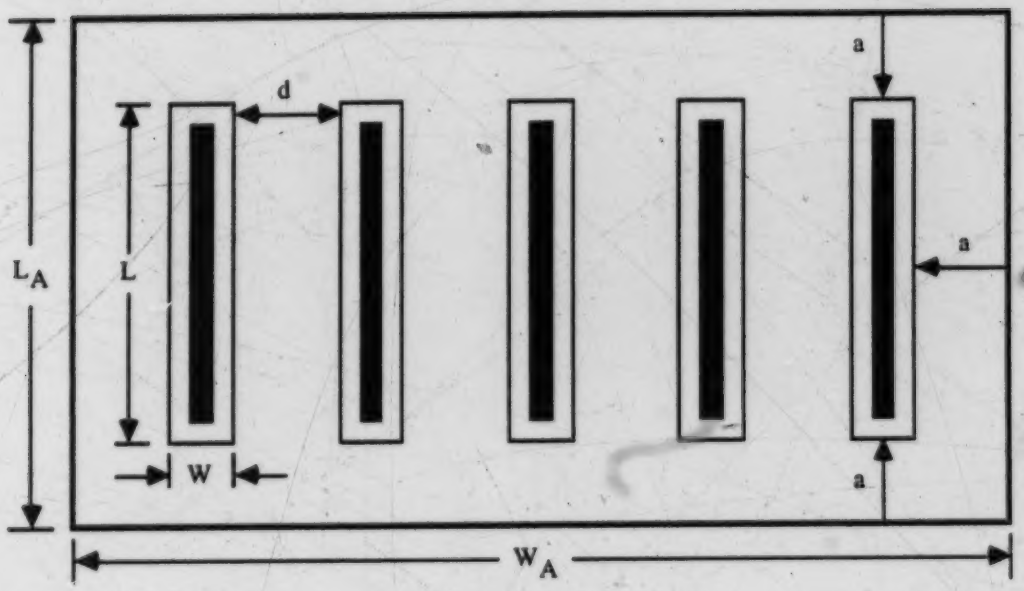

Fig. 3.3 Dimensions of the VHD geometry.

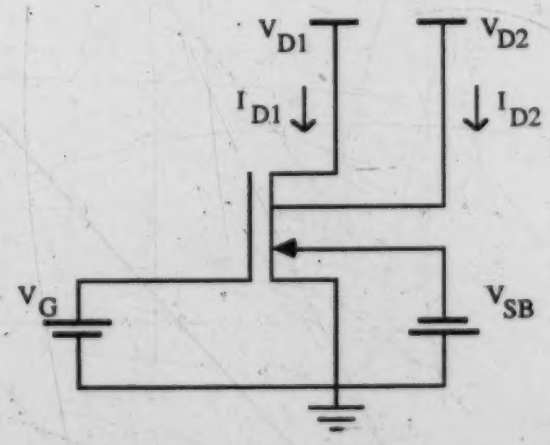

Fig. 3.4 General biasing configuration of the dual drain MAGFET.

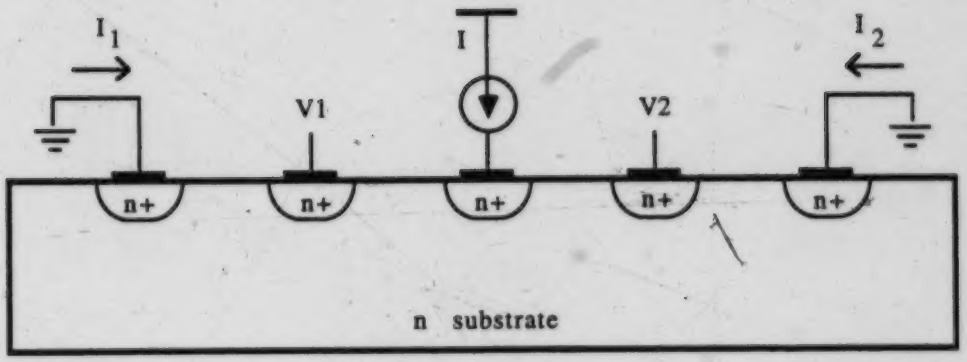

Fig. 3.5 General biasing configuration of the VHD.

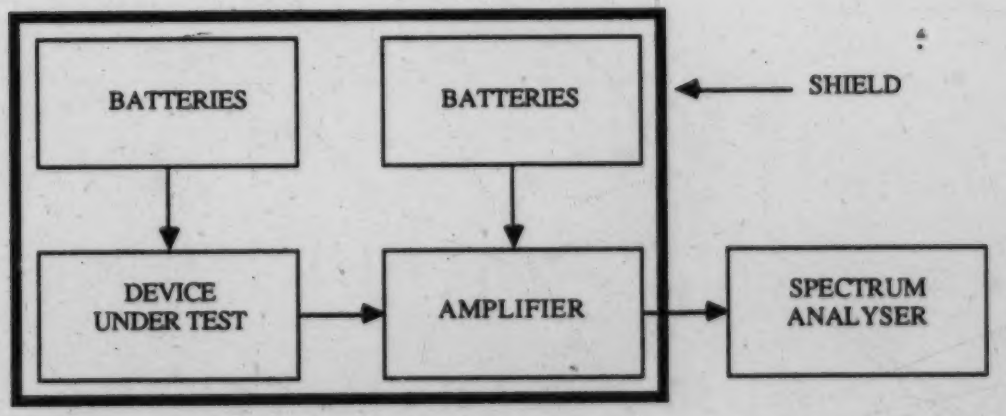

Fig. 3.6 Experimental setup for noise measurements.

Table 3.1 Frequency range and number of averaged readings

Frequency range (Hz)	.1-10	10-100	1-100	100-1k	1k-10k	10k-100k
Number of averages	100	300	500	2000	5000	5000

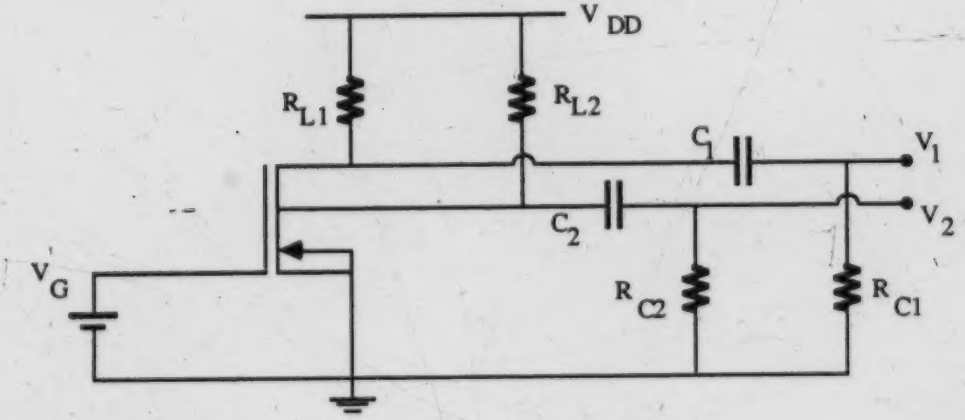

Fig. 3.7 Biasing and high pass filtering circuit for performing noise measurements on the dual drain MAGFETs.

Table 3.2 Load resistances for MAGFET noise measurements

MOS operating region	Linear	Saturation		
Device geometry (W/L)	100/100	100/100	100/25	25/100
Drain load resistance when both drains operating.(k ohms)	100	33.2	13.7	147.5
Drain load resistance when other drain floating. (k ohms)	—	21.5	10.0	78.5

4. MAGFET RESULTS

4.1 Microtel Pacific Devices

The graphs in Figs. 4.1 to 4.15 are typical plots of the relative current imbalance for the various dual drain MAGFETs fabricated via the Microtel Pacific process. The graphs in Figs. 4.1 to 4.5 demonstrate the dependence of the relative current imbalance at B=1 T on V_{DS} for various V_{GS}, while for Figs. 4.6 to 4.10 the dependence is with respect to V_{GS} for various V_{DS}. The graphs in Figs. 4.11 to 4.15 represent device response to magnetic field for various operating points. At each gate voltage indicated the drain to source voltage was 5.0 V. In each case the different devices are operated over identical ranges of biasing voltages and field strengths.

4.1.1 Discussion

Considering only the n-channel MAGFETs we can say that the overall percentage imbalance increases with increasing length to width ratio of the device. The same relationship appears from the numerical modelling of this structure [2], and from equation (2.8) for wide devices;

$$\delta(B) = I_H / I = (L/W)\mu^* B. \qquad (4.1)$$

Comparison of the two square geometries reveals the effects of scaling the devices width, length and drain separation, (see Figs. 4.1 and 4.2). Although the average response is about the same for both sizes the range of

sensitivity of the smaller 25 μm square MAGFET is noticeably larger. For the smaller square MAGFET the slopes of the lines of constant gate voltage are higher, and the separation between lines of constant gate voltage is greater. Determining a probable physical cause for the latter is difficult. In each device the gate induced field is the same. Scaling the device size merely scales the current density in the channel. The higher slope values are probably caused by the drain to source voltage. Shorter channels result in higher longitudinal electric fields. In bulk silicon drift mobility decreases with higher electric field [27]. If this idea is extended to surface layers with the Hall and drift mobility related by a constant scattering factor over this range of electric field strength, then negatively sloped lines would be expected, not the positively sloped lines we see here. In this sense there is no means by which a higher electric field could enhance the Hall mobility. However, it must be remembered that the density of charge in the inversion layer is dependent on the voltage along the channel, being higher for a lower voltage [25]. Thus the variation of mobile charge density along the length of the channel is more pronounced in the smaller square MAGFET at any given drain to source voltage. Further complicating the variation of channel charge density is the Hall voltage generated across the width of the device. The theoretical analysis of any magnetically sensitive MOS structure is usually confined to situations where the drain to source voltage is low. This ensures a virtually uniform channel which simplifies the problem. Unfortunately there is no indication in the literature as to how a non-uniform channel could affect the device response.

The picture becomes very complicated when V_{DS} is increased enough to produce pinch-off. The inversion layer length decreases by virtue of the

depletion region formation at the drain end. For the smaller square MAGFET this means a greater percentage change from the original channel length. On the basis of the equation (4.1), decreasing the channel length should decrease the response. Channel shortening by V_{DS} is inconsistent with this fact since the opposite effect occurs. Then too it must be remembered that the current must also pass through the depletion region under the influence of the magnetic field. An analysis could then proceed on the basis that there is a region of high Hall mobility adjoining the end of the inversion layer. This would definitely explain the positive slope of the curves. However, if the current deflection is an end effect like the magneto-resistance of long Hall plates [7], it is a gross simplification which could lead to fictitious results.

The two remaining NMOS MAGFETs, the wide and long channel devices, exhibit basically the same characteristics as the two square MAGFETs. Their degree of dependence on V_{DS} is worth noting. The long channel MAGFET has a greater dependence on the drain to source voltage than the short channel MAGFET. Since the 25 μm square and wide channel devices have the same channel length they suffer the same degree of channel shortening from V_{DS}. By comparison the percentage change in the channel length of the long channel MAGFET is not as great, and it would be expected that the relative imbalance should not increase as much with V_{DS}. This discrepancy can be reconciled by considering whether the current imbalance is an end effect or not. Consider the current and equipotential lines for the two extreme Hall plate geometries, the very long plate and the very wide plate, (see Fig. 2.2). The long geometry has current lines running parallel to the sides of the device, except when near the ends, thus current imbalance is

predominantly an end effect. For the wide geometry the current lines are generally angled to the sides except when very near them. Thus carrier deflection occurs fairly equally throughout the device, and current imbalance is not an end effect. Applying this to the long channel MAGFET we see that the depletion region formation could have a great influence on response since most of the current deflection could occur within it. Hence a greater dependence on V_{DS} results. The wide channel MAGFET is not influenced to the same degree by the formation of the depletion region since the current deflection does not occur for the most part at the ends, resulting in a smaller dependence on V_{DS}.

Compared to the NMOS MAGFETs the PMOS has a lower relative imbalance. However, the group of curves for either type of MAGFET behave similarly. The average response of the PMOS MAGFET is about half that of the wide NMOS MAGFET. If the channel is wide enough for us to assume that the imbalance is proportional to the aspect ratio, then the response of a 100 μm x 25 μm PMOS MAGFET should be about 25% less then that of a 75 μm x 25 μm PMOS. The response of the same size NMOS is then approximately 2.5 times larger. Since the relative imbalance is a measure of the Hall mobility, the ratio of electron to hole Hall mobility in the inversion layer is then similar to the ratio of electron to hole drift mobility in bulk silicon.

The dependence of relative current imbalance on gate voltage is more clearly shown by graphs 4.6 to 4.10. Comparing the graphs of the two square NMOS MAGFETs we can see that scaling has little effect on the occurrence of maximum response at V_{GS}≈1.7 V. Note that for the smaller square MAGFET the peak is more pronounced, and as shown from the previous graphs the

dependence on V_{DS} is greater. For the wide and long channel devices the peaks are respectively at V_{GS}=2.2 V and V_{GS}=2.6 V. These data yield no simple relationship between geometry and the gate voltage of maximum response. The PMOS MAGFET also has a peak in response, at V_{GS}=-1.2 V. The typical threshold voltages are 0.8 and -0.6 V for the NMOS and PMOS devices respectively. Thus the peaks occur at gate voltages of about twice the threshold voltage or more.

This peaking phenomenon could be a consequence of the screening effect. Numerical verification would require a knowledge of the density of Coulomb scattering centres. It must also be remembered that these plots are proportional to, or at least more indicative of, Hall mobility, whereas the screening theory was developed for drift mobility. Furthermore if the curves for the different geometries were more similar and the peaks occurred nearer the same gate voltage, then at first glance this explanation would be more believable.

When exposing any of these devices to a varying magnetic field we can see from Figs. 4.11 to 4.15 that the relative imbalance, within the accuracy of the experiment, is essentially a linear function of field strength. The deviation of the measured data from the computed best fit lines is usually less than 1%. This is using expression (2.14) for $\delta(B)$. With the current imbalance normalized to the total current at zero field the deviation from a best fit line is also well within the measurement error. The percentage deviations of each datum point from a best fit straight line using these two definitions of $\delta(B)$ seldom differ by more than a few tenths of a percent. Some lines do not pass through the origin because of offset currents. Much of the bias

dependence of the relative imbalance which was observed in the previous graphs can also be seen in these graphs. Thus for field strengths of up to one Tesla the MAGFET, in terms of relative current imbalance, is virtually a linear sensor. Provided that the offsets can be made negligible, it is also symmetric in the relative current imbalance.

4.2 Northern Telecom Devices

The graphs in Figs. 4.16 to 4.30 are typical plots of the relative current imbalance for the MAGFETs fabricated via the Northern Telecom process. The graphs in Figs. 4.16 to 4.20 demonstrate the dependence of the relative current imbalance at B=1 T on V_{DS} for various V_{GS}, while for Figs. 4.21 to 4.25 the dependence is with respect to V_{GS} for various V_{DS}. The graphs in Figs. 4.26 to 4.30 represent device response to magnetic field for various operating points. At each gate voltage indicated the drain to source voltage was 5.0 V. In each case the different devices are operated over identical ranges of biasing voltages and field strengths. The range of biasing conditions and magnetic field strengths are the same as for the Microtel samples.

4.2.1 Discussion

Again we start by considering the n-channel MAGFETs, (Figs. 4.16 to 4.19). For a preliminary comparison we use the percentage imbalance at the centroid of the area bounded by the curves. The centroid is approximated visually. This results in an imbalance of 1.2% for the wide channel MAGFET, 4.8% for the 100 μm x 100 μm MAGFET, 5.2% for the 25 μm x 25 μm MAGFET, and 6.0% for the long channel MAGFET. Thus the relative imbalance increases

with increasing length to width ratio (L/W). The ratio of the relative imbalance of the square devices to the wide device is about 4. This is exactly the ratio of their L/W ratios. The long channel MAGFET also has an L/W ratio 4 times larger than the square MAGFETs. However its relative imbalance is only about 1.2 times larger. This indicates that eventually little improvement in the relative imbalance can be had by continually increasing the length to width ratio.

The two square geometries realized by this process unfortunately can not be strictly compared. In the design of the 25 μm x 25 μm MAGFET, a contact cut to the substrate contact was omitted. Thus the results shown here are for the source floating with respect to the substrate. Even under this condition the numerous devices tested show remarkably similar results. Among these is the anomaly at V_{GS}=1.0 V and V_{DS}=3.0 V, which is most likely caused by this design error.

An interesting point to note about the graph for the long channel MAGFET is the behaviour of the curves in the MOS linear region of operation, (see Fig. 4.19). Consider the curve for V_{GS}=5.0 V and V_{DS}<4.0 V. As the drain to source voltage increases from its near zero values the relative imbalance curves upward. Further increases in the drain to source voltage decrease the rate of increase of the current imbalance. From V_{DS}=3.0 V to the pinch-off voltage of 4.0 volts the rate of increase is fairly constant. This straight line behaviour of the relative current imbalance continues into the saturation region. The saturation region comprises a small portion of the V_{GS}=5.0 V curve, hence this particular observation is more obvious in the lower gate

voltage curves. These described characteristics are common to most of the long channel devices tested, and also to the square channel devices. Some devices start with unusually high relative imbalance at low drain to source voltages, however as V_{DS} approaches 1.0 V the response follows this particular pattern. A possible explanation for this behaviour in the linear region could lie in the influence of the drain to source voltage on the inversion layer. As V_{DS} increases, causing the carrier concentration along the channel to become less uniform, an increase in relative imbalance from the more uniform case could result. Again, owing to the complexity of the problem, such claims are difficult to substantiate analytically.

The PMOS MAGFET has a rather large relative imbalance, (see Fig. 4.20). In this figure the V_{GS}=-1.0 V curve is not plotted since the device threshold voltage is approximately -1.1 V. From the curves shown we can assign a typical imbalance of 1.2% to the PMOS MAGFET. This is almost the same as the wide channel NMOS. If we are to assume again that the aspect ratio of 3:1 is applicable in equation (4.1) this results in a relative imbalance of 0.9% for an aspect ratio of 4:1. This figure is still comparable with that of the wide channel NMOS MAGFET. This indicates that for the Northern Telecom process the hole Hall mobility is quite close to the electron Hall mobility.

For the Northern Telecom devices, the behaviour of the relative imbalance with respect to gate voltage is similar to that of the Microtel Pacific devices, (see Figs. 4.21 to 4.25). All the MAGFETs exhibit a peak in relative imbalance at a particular gate voltage, which is influenced to a degree by the drain to source voltage.

The large square MAGFET has a maximum in sensitivity at V_{GS}=1.5 V, (see

Fig. 4.21). The magnitude of the peak increases marginally with increasing drain to source voltage, while the location of the peak is for all purposes unaltered. The smaller square MAGFET has a peak at V_{GS}=1.5 V at low drain to source voltages, (see Fig. 4.22). The location and magnitude of the peak are more affected by V_{DS}, but this can not all be attributed to scaling since the source is not tied to the substrate in this device. The measured threshold voltage of the large MAGFETs is typically 0.9 V. All the data in the graph is for the MAGFET operating in the MOS saturation region. However, by analysing the graphs of the relative imbalance versus V_{DS} it can be seen that the peaking occurs from the linear region through to the saturation region.

The peak in relative imbalance for the wide and long channel MAGFETs occur respectively at V_{GS}=1.5 V and V_{GS}=2.0 V, (see Figs. 4.23 and 4.24). The effect of V_{DS} on the location of the peaks is harder to establish for these devices. The curves of constant V_{DS} for the wide channel MAGFET are not very smooth and for the long channel MAGFET the peaks are quite broad. For both devices the magnitude of the peak increases with increasing drain to source voltage. Again, for the indicated range of biasing voltages the peaks all occur in the MOS saturation region. As for the square MAGFET, the corresponding graphs of relative imbalance versus drain to source voltage also show that the peaking exists throughout the entire operating range.

The PMOS MAGFET graph of relative imbalance versus gate to source voltage is similar to that of the wide channel MAGFET, (see Fig. 4.25). The peak occurs at V_{GS}=-1.5 V. Increasing the magnitude of V_{DS} increases the magnitude of the peak, but has no apparent effect on its location.

The typical threshold voltages are 0.9 V for the NMOS and -1.1 V for the PMOS devices. Thus in this process the peaking occurs for gate voltages 1.5 to 2.0 times larger than V_T.

For all the Northern Telecom devices $\delta(B)$ is essentially linear, using either $[I_1(B)-I_2(B)]/[I_1(B)+I_2(B)]$, or $[I_1(B)-I_2(B)]/[I_1(0)+I_2(0)]$, as the definition of $\delta(B)$. The data points usually deviate less than 1% from a best fit line. For each datum point the percentage deviations from a best fit line, in the two cases, usually differ by a few tenths of a percent.

4.3 Comparison

We compare the MAGFETs realized in the Northern Telecom and Microtel Pacific technologies in terms of device response averaged over the number of samples available. Graphs 4.31 to 4.40 are the averaged percentage current imbalance versus V_{DS} for the five dual drain MAGFETs. For the Microtel process 9 samples of each square MAGFET were available, while 8,6 and 7 samples were available for the wide long and PMOS MAGFETs respectively. For the Northern Telecom process 10 samples of each type of dual drain MAGFET were available.

Starting with the square channel MAGFETs it can be seen that the general behaviour of the group of curves from the two processes is quite similar. The standard deviation from the average is typically 1%, except at points of low V_{DS} and V_{GS} where it is usually better than 5%,. No doubt this is a reflection of the standardization of the CMOS process. For both square geometries, (see Figs. 4.31, 4.32, 4.36, and 4.37), the Northern Telecom process gives the higher relative imbalance.

The long channel devices are also very similar, (see Figs. 4.34, and 4.39). For the Microtel process the standard deviation is about 10% of the average at V_{GS}=2.0 V and drops to about 6% at V_{GS}=5.0 V. At a gate voltage of 1.0 volt, which is slightly more than the threshold voltage the deviation is typically 15%. The Northern Telecom samples, start with a standard deviation of about 6% at V_{GS}=1.0 V dropping to 2% at V_{GS}=5.0 V. Here too the Northern Telecom samples have the higher relative imbalance.

For the wide channel devices in the Microtel process the standard deviation starts at about 20% of the average at V_{GS}=1.0 V. At V_{GS}=2.0 V it drops to about 3% and rises to 6% at V_{GS}=5.0 V, (see Fig. 4.33),. The Northern Telecom devices have a standard deviation of about 7% at V_{GS}=1.0 V and for larger gate voltages it remains better than 3%, (see Fig. 4.38). As for the previously mentioned devices the relative imbalance of the Northern Telecom devices is greater.

The PMOS MAGFETs realized in these two technologies give markedly different results. The Microtel samples have a typical standard deviation of 15%, rising to 20% at V_{GS}=-1.0 V, (see Fig. 4.35). The Northern Telecom samples have a variation of about 2%, while for V_{GS}=-1.0 V the data is not valid since the threshold voltage is not reached, (see Fig. 4.40). Most astonishing is the difference in their relative imbalance. Northern Telecom samples have about twice the relative imbalance of the Microtel samples. Inspection and repetition of the experimental procedure did not change this result.

The relative imbalance at 1.0 Tesla with respect to gate to source voltage

is also compiled statistically, (Figs. 4.41 to 4.50). For the Microtel process the number of available devices were, six 100 μm x 100 μm MAGFETs, three 75 μm x 25 μm PMOS, and five each of the rest. Ten samples of each device were available from the Northern Telecom process. With regards to the magnitude of the relative imbalance and its standard deviation the same can be deduced as was done from the previous graphs. In general the relative imbalance is higher and the standard deviation is less for the Northern Telecom samples. Another obvious quantity to compare from these graphs is the value of gate voltage at which the peak relative imbalance occurs. For any of the devices this particular value of gate voltage is not the same in both processes. The closest they come to coinciding is for the 100 μm x 100 μm MAGFET, where the peaks are at 1.6 V for the Microtel samples, (see Fig. 4.41), and 1.4 V for the Northern Telecom samples, (see Fig. 4.46). The next closest is the PMOS MAGFET with the peaks occurring at -1.2 and -1.5 volts, (see Figs. 4.45 and 4.50). The peaks in the remaining devices differ by 0.5 V or more. Even if the peaks are compared in terms of $(V_{GS}-V_T)$, the resulting voltage values for any given device are not equal for the two processes. A consistent fact about the peaks is that they occur at lower gate voltages for the n-channel Northern Telecom devices. The same is true for the P-channel MAGFET, that is at a higher negative gate voltage. Thus the phenomenon is not only geometry dependent but also process dependent.

As a whole the Northern Telecom process results in NMOS MAGFETs which are marginally better, and PMOS MAGFETs which are substantially better in terms of relative current imbalance. Just as important is the consistency of response for samples of identical design. With regard to

standard deviation from the average the Northern Telecom process performs as well or better than the Microtel process.

4.4 Current Imbalance and Source to Substrate Voltage

In integrated MOS circuits the condition can arise where a voltage difference exists between the source and substrate of a MOSFET. The voltage reverse biases the diode formed by the source and substrate diffusions, causing the isolating depletion region to thicken. The major effect of the source to substrate voltage is an increase of the device threshold voltage [25]. A MAGFET with supporting on chip circuitry may have a source to substrate voltage, hence it is necessary to investigate the relationship between the current imbalance and the source to substrate voltage. For this purpose the MAGFET is biased as shown in Fig. 3.4. One device of each dual drain geometry is tested, both in the MOS linear and saturation region. The devices used are from Northern Telecom.

At zero source to substrate voltage a peak in relative imbalance with respect to gate voltage is observed. This peaking phenomena persists with a non zero source to substrate voltage, whether the device is operated in the saturation or linear region. The graphs is in Figs. 4.51 to 4.54 are the results from tests in the saturation region. The two drain to source voltages are maintained at 5.0 V. In terms of $(V_{GS}-V_T)$ the source to substrate voltage affects the magnitude of the peak but not the point at which it occurs. Generally the relative imbalance decreases as the magnitude of V_{SB} increases. This is understandable in terms of the electric field strength perpendicular to the MOS channel. As V_{SB} increases, causing the threshold

voltage to increase, the gate to source voltage required to create the inversion layer increases. The result is higher transverse electric fields in the inversion layer, which are known to degrade the drift mobility [20, 28]. Thus the Hall mobility, being related to the drift mobility by the scattering factor, should degrade as well, causing a lowering of the relative imbalance.

Since the peaks occur at $|V_{GS}-V_T| \geq 0.5$ V, the linear region V_{DS} bias point is arbitrarily chosen as 0.3 V. The results in the linear region are similar to those of the saturation region. Again V_{SB} decreases the magnitude of the peaks but does not affect their placement in terms of $(V_{GS}-V_T)$, (Figs. 4.55 to 4.58). Comparing the results in the saturation region to those in the linear region we note that for any device the peaks occur at practically the same value of $(V_{GS}-V_T)$. The largest discrepancy being for the wide channel MAGFET, however the peak broadens considerably in the linear region. The currents in the linear region are quite low, making determination of current differences more prone to experimental inaccuracy. This problem is alleviated to a degree by operating the analyser at longer integration times. The integration time refers to the number of instantaneous readings that are averaged to reduce errors from device noise and external electromagnetic interference.

Since the occurrence of the peaks in both regions is coincident in terms of $(V_{GS}-V_T)$, it appears that Hall mobility is dependent on carrier density in the inversion layer, the carrier density being proportional to $(V_{GS}-V_T)$ [25]. At low drain to source voltages the variation of carrier concentration along the channel length is small. It is then surprising to

have the peaks at the same $(V_{GS}-V_T)$ in the saturation region since the carrier concentration varies drastically from drain to source. This apparent problem can be clarified by considering the various field strengths in the conducting channel [20, 21]. Although for a fixed gate and substrate bias the carrier concentration along the channel length can vary with V_{DS} the normal electric field is essentially independent of channel position. Provided that the longitudinal electric field from V_{DS} is much smaller than the perpendicular electric field the total field does not change much with V_{DS}. Hence, with mobility dependent on electric field we would expect little change in the behaviour of the relative imbalance with V_{DS}.

The graphs in Figs. 4.51 to 4.58 are plotted with $(V_{GS}-V_T)$ as the independent variable to demonstrate the condition for which the peaks coincide with varying V_{SB}. To better see how the relative imbalance at fixed gate and drain voltages varies with V_{SB} we turn our attention to Figs. 4.59 to 4.66. For all the devices, whether biased in the saturation or linear region, the relative imbalance can drop off drastically with increasing $|V_{SB}|$. This occurs at low gate to source voltages. Since $|V_T|$ increases with $|V_{SB}|$ the devices eventually turn off. For higher gate to source voltages, several volts greater than V_T, the devices are not at risk of being turned off, even up to $|V_{SB}|$=5.0 V. In this case we can see that the relative imbalance changes very little with V_{SB}, whether the device is biased in the MOS linear or saturation region. Over the range of V_{SB} indicated, with the devices operating at fixed

gate and drain voltages in the MOS saturation region, δ changes less than 10%.

4.5 The Triple Drain MAGFET

The triple drain MAGFETs are subject to some of the same tests as the dual drain MAGFETs. The general response of the triple drain MAGFET is quite similar in nature to the response of the 100 μm x 100 μm dual drain MAGFET. The graph in Fig. 4.67 is for a Microtel sample. The slopes of the curves of constant gate voltage and the degree of their separation are about the same as for the large square dual drain MAGFET. As with all the other MAGFETs here too the peaking of response with respect to gate voltage can be seen. The V_{GS}=1.0 V curve is the lowest while V_{GS}=2.0 V is the highest and then falling for $V_{GS} \geq 3.0$ V. Thus somewhere between 1.0 and 3.0 volts there is a peak. The peaking exists from the linear region into pinch-off and through to the saturation region. In terms of relative current imbalance the important thing to note is that for any given bias point the triple drain structure has a greater relative imbalance than the dual drain structure. Using the centroid of the area bounded by the gate voltage curves as a means of quick comparison, the dual drain MAGFET has a relative imbalance of about 4.2% and the triple drain 6.2%.

The triple drain MAGFET thus shows, as was expected from modelling results [12], a better relative imbalance than the dual drain square MAGFET. This result though can be affected by the definition of current imbalance used. For the graph in Fig. 4.67 the plotted percentage imbalance is as per equation (2.14), where I_1 and I_2 represent the current in the two outer

drains. For the graph in Fig. 4.68 the following definition is used;

$$\delta=(I_1(B)-I_2(B))/(I_1(B)+I_2(B)+I_3(B)) . \qquad (4.2)$$

The imbalance of the two exterior drains is normalized to the sum of the current through the three drains. This is reminiscent of the previous definition of relative imbalance as applied to the dual drain devices. The third drain produces some ambiguity, but its inclusion into the definition seems reasonable. The data used in both of these latest graphs are all from the same test. The curves as before behave in the same fashion. Using the centroid technique described earlier we arrive at a relative imbalance of 3.5%, almost 20% lower than that of the dual drain MAGFET.

If it were possible to inject large currents into the middle drain while keeping the currents in the outer drains relatively small very high figures of relative imbalance could be obtained with equation (2.14), whereas equation (4.2) would render figures similar to those measured here. Establishing such a condition in a triple drain MAGFET is not straightforward. If the device is in saturation then the drain currents saturate. Lowering the voltage of the outer drains would decrease the current flow through these drains, but eventually additional current components would flow from the voltage difference between the middle and outer drains. Another approach would be to make the middle drain larger and the outer drains smaller, but minimum size is limited by the process. As well, this would certainly produce larger offsets. If by any of these methods higher relative imbalance figures could be reached, the actual current difference would not be all that different from that of the triple drain or dual

drain structures used here.

The triple drain MAGFETs made with the Northern Telecom process present no new revelations. The peak with respect to the gate voltage is again evident. The relative imbalance in Fig. 4.69 is calculated from the outer drain currents using equation (2.14). The overall relative imbalance is about 7%, slightly better than the Microtel sample, and consistent with the results of the dual drain MAGFETs.

4.8 Mobility Results and Discussion

Using the outlined procedure, the Hall mobility, drift mobility, and corresponding scattering factor have already been determined for the n type inversion layer of the Microtel Pacific devices [24]. The major findings are that the electron scattering factor is greater than one, and that for strongly inverted surfaces it is practically constant. The geometric factors K, (see equation 3.2), determined using the numerical modelling program Albertina are respectively .56, .15, and .64 for the square, wide, and long geometry [24].

For the Northern Telecom process three devices of each geometry, large square, wide, and long channel are tested. These devices are from the same batch used in the magnetic sensitivity measurements. The mobilities and scattering factor of a 100 μm x 100 μm, and 100 μm x 25 μm dual drain MAGFET are shown in Fig. 4.70 and 4.71 respectively. Except for the wide geometry, once the surface is strongly inverted, i.e. $V_{GS} \geq 2.0$ V, the scattering factor usually varies less than ±5% from a mean value. All the wide channel MAGFETs tested exhibit a scattering factor that increases smoothly with gate voltage. The $V_{GS}=5$ value of r_n is about 20% more than the $V_{GS}=2$ value of r_n.

Since the C'_{ox} value is not measured and the geometric factors K have not been verified by other means, the accuracy of r_n is unknown.

A striking feature of the drift mobilities in Figs. 4.70 and 4.71 is the behaviour of the ratio μ(square)/μ(wide) for the indicated gate voltage range. Provided that C'_{ox} of each device on the same chip doesn't vary much, this ratio should be near one and constant. For all the wide devices tested this ratio is about 1.2 at V_{GS}=2.0 V, and rises to 1.5 at V_{GS}=5.0 V. Why the ratio rises is not clear. This behaviour may be the cause of r_n increasing with gate voltage. A simple explanation may exist for this ratio not being near one. In equation (3.3) the W/L ratio is that of the outside width and length of the MAGFET channel. The wide MAGFET has a drain separation of 20 μm which is comparable to the channel length of 25 μm. Intuitively one would expect that because of the relative size of these dimensions the actual W/L ratio should be less than 4/1. If this is true the calculated drift mobility of the wide MAGFET would increase, lowering the ratio μ(square)/μ(wide). The ratio μ(square)/μ(long) is typically 1.04 ±.02, which is closer to what is expected. The square and long devices have a channel length to drain separation ratio of 5 and 20 respectively. Thus if MAGFETs are to be used in determining inversion layer drift mobility it would be advisable to keep the channel length to drain separation ratio as large as possible, otherwise a geometric correction factor would be required. If it can be assumed that the W/L ratios of the long and square MAGFETs are correct, then to obtain μ(square)/μ(wide)=1 the W/L ratio of the wide MAGFET would have to be

reduced approximately 20% to 3.2/1.

The Hall mobility ratios μ^*(square)/μ^*(wide) and μ^*(square)/μ^*(long) are both fairly constant for each group of devices on the same chip. They vary about ±2% from the mean when the channel is strongly inverted. The typical values are μ^*(square)/μ^*(long)≈.97, which is near the anticipated value of 1, and μ^*(square)/μ^*(wide)≈1.17, which could be improved upon. The Hall mobility calculation is based on equation (3.2) and knowing the value of K. If the geometric factors of the square and long MAGFETs are correct then K=.15 for the wide MAGFET would have to be decreased approximately 17% to .125. This would increase μ^*(wide), bringing μ^*(square)/μ^*(wide) closer to unity.

Regarding Fig. 4.70 and the mobility curves we see that the peaks do not coincide. For the drift mobility the location, and even the existence of the peak is dependent on the values of V_T and $(1/2+(\varepsilon_s q N_A/|\psi_B|)^{1/2}/4C'_{ox})$ used in equation (3.3). If either of these quantities is increased the magnitude of the peak increases and shifts to the left, i.e. lower gate voltages. Actually the entire drift mobility curve will increase at each gate voltage point, however the increase will be less noticeable at higher gate voltages. With the peak increasing and shifting to the left the scattering factor will flatten out at lower gate voltages, extending the range of almost constant behaviour.

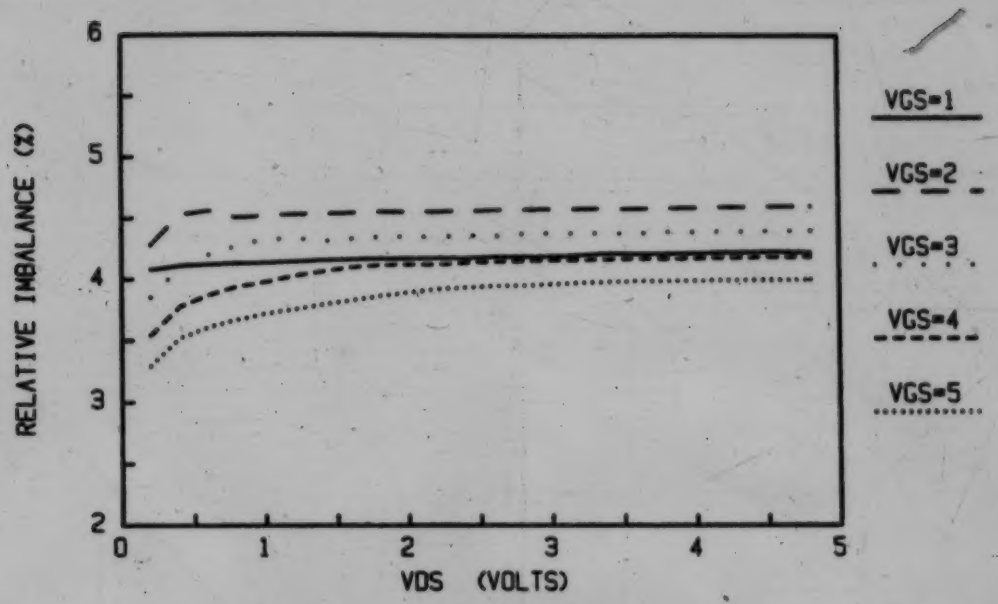

Fig. 4.1 Relative current imbalance (%) at 1 Tesla as a function of operating point for the square MAGFET (W/L=100μm/100μm), fabricated via Microtel Pacific.

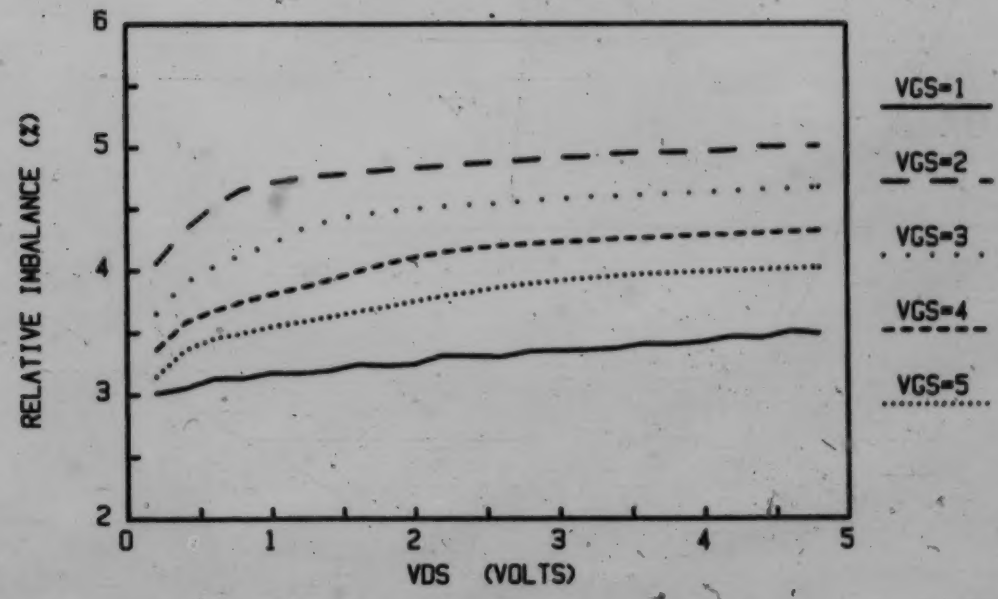

Fig. 4.2 As in Fig. 4.1, but for the square MAGFET (W/L=25μm/25μm).

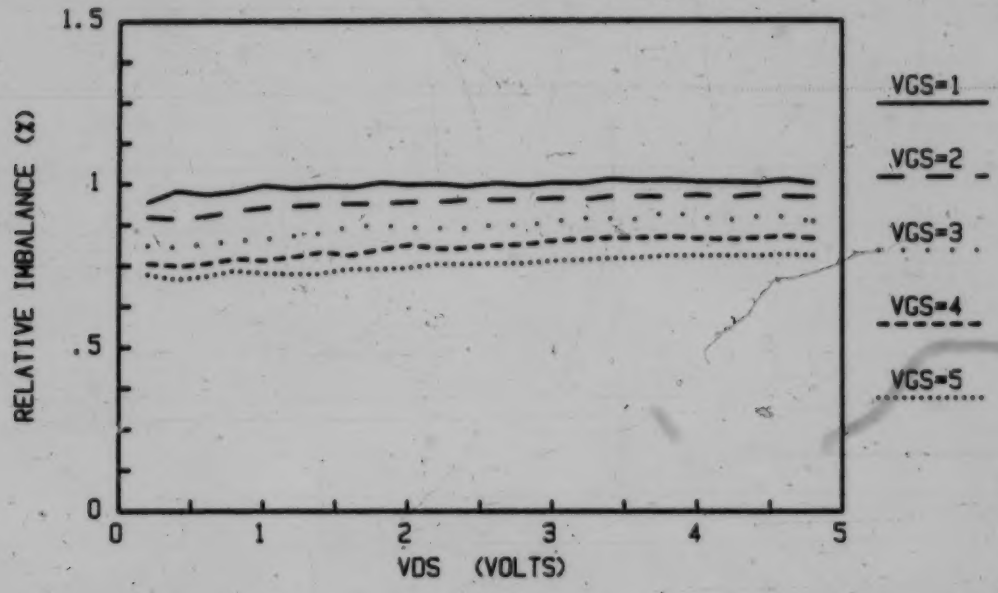

Fig. 4.3 As in Fig. 4.1, but for the wide MAGFET (W/L =100μm/25μm).

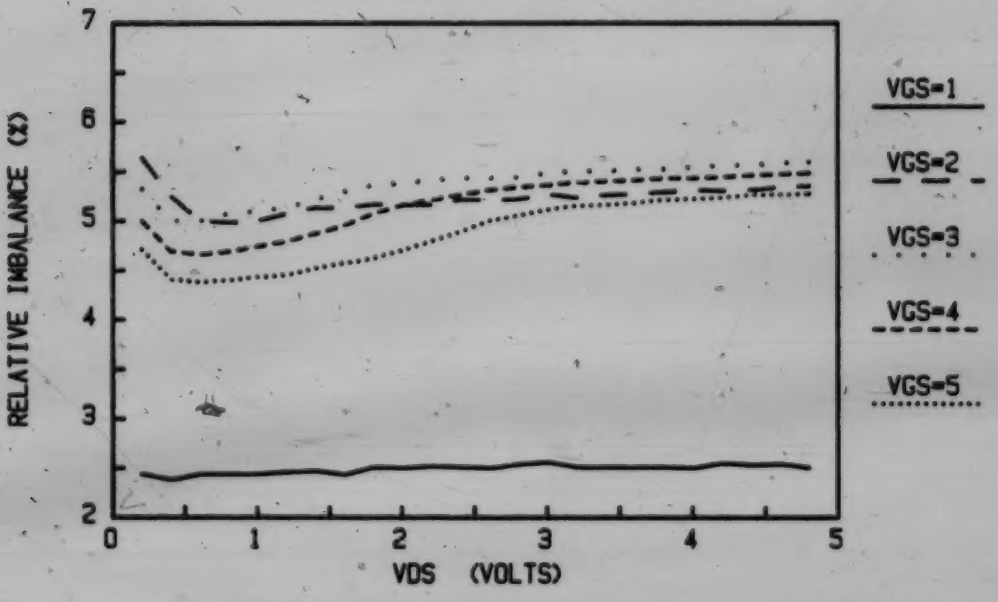

Fig. 4.4 As in Fig. 4.1, but for the long MAGFET (W/L=25μm/100μm).

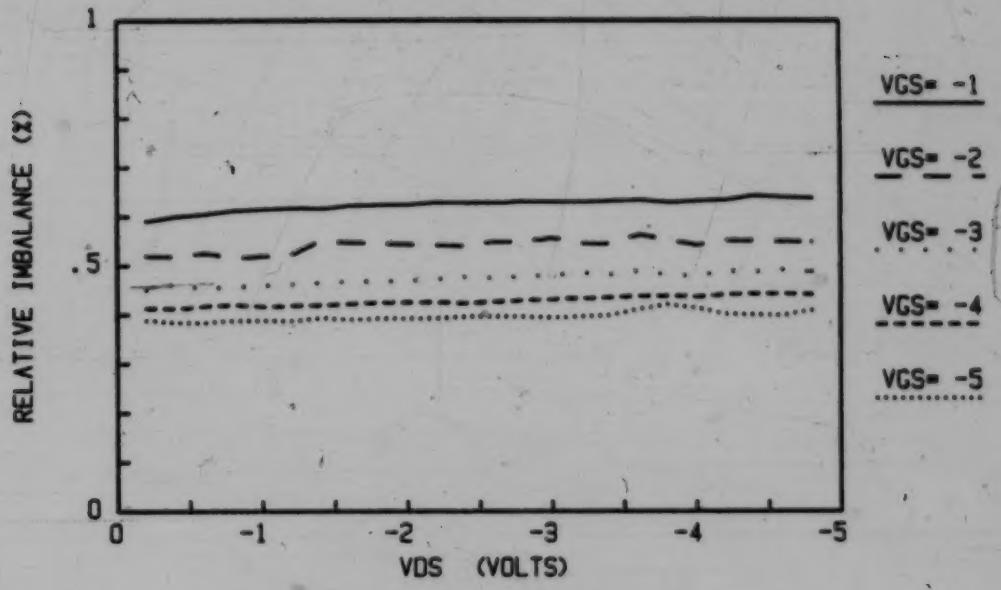

Fig. 4.5 As in Fig. 4.1, but for the PMOS MAGFET (W/L=75μm/25μm).

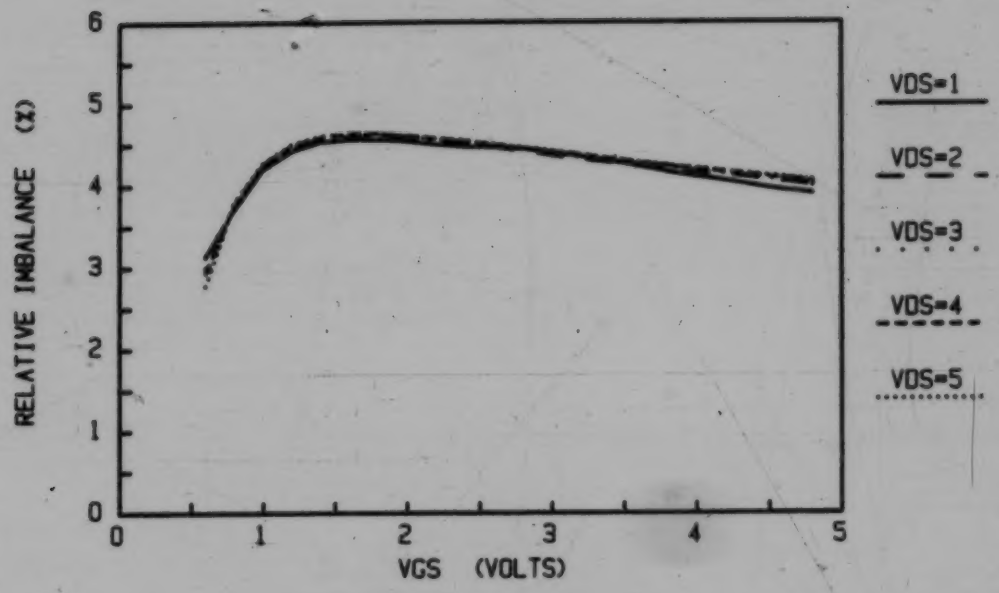

Fig. 4.6 Relative current imbalance (%) at 1 Tesla as a function of operating point for the square MAGFET (W/L=100μm/100μm), fabricated via Microtel Pacific.

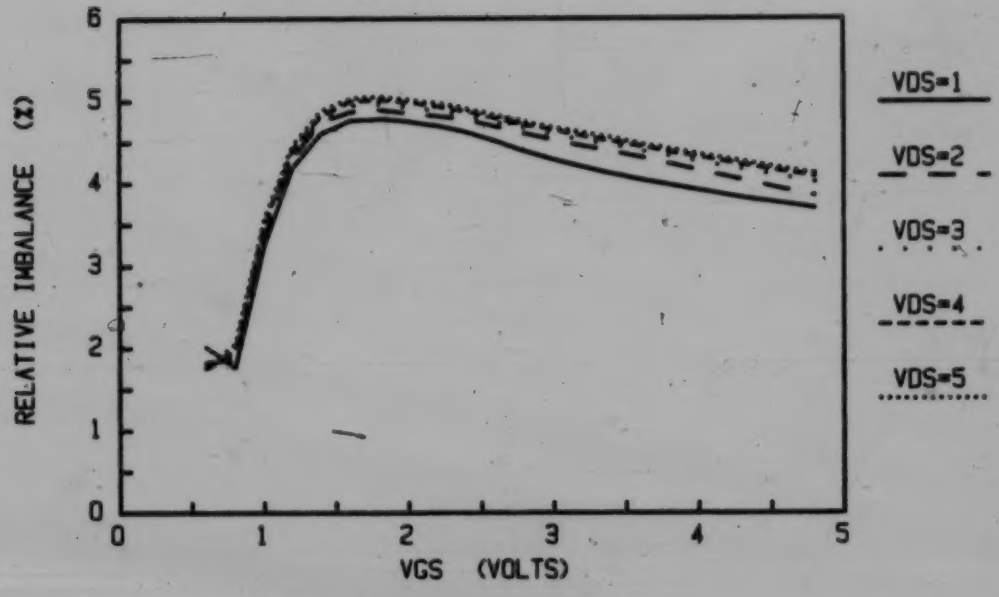

Fig. 4.7 As in Fig. 4.6, but for the square MAGFET (W/L=25μm/25μm).

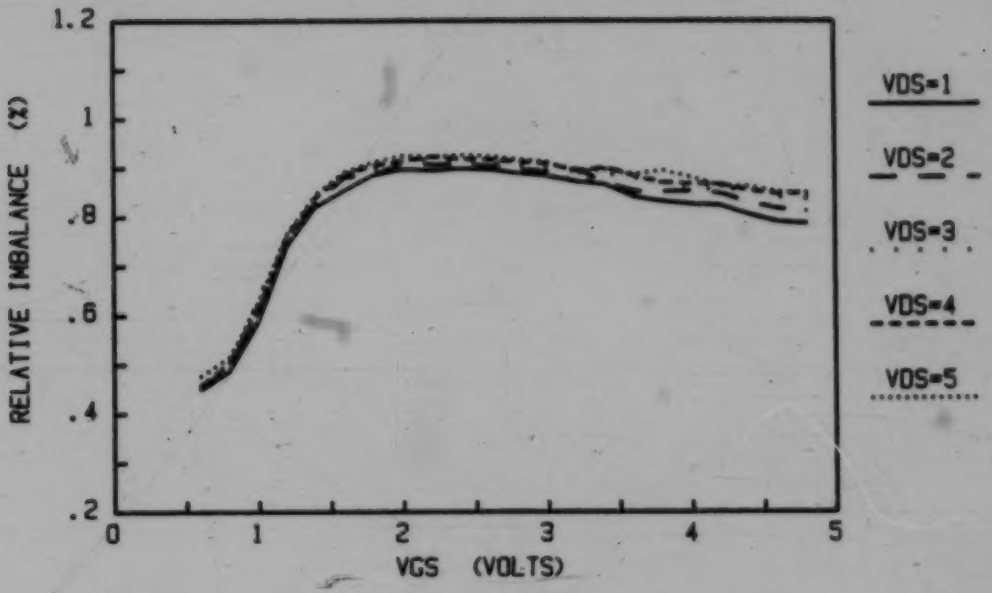

Fig. 4.8 As in Fig. 4.6, but for the wide MAGFET (W/L=100μm/25μm).

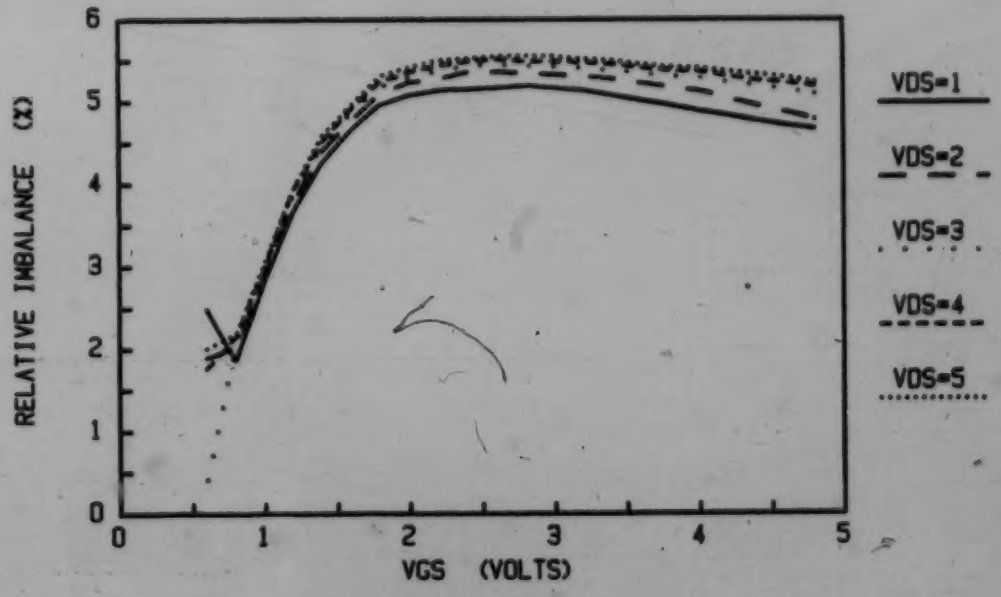

Fig. 4.9 As in Fig. 4.6, but for the long MAGFET (W/L=25μm/100μm).

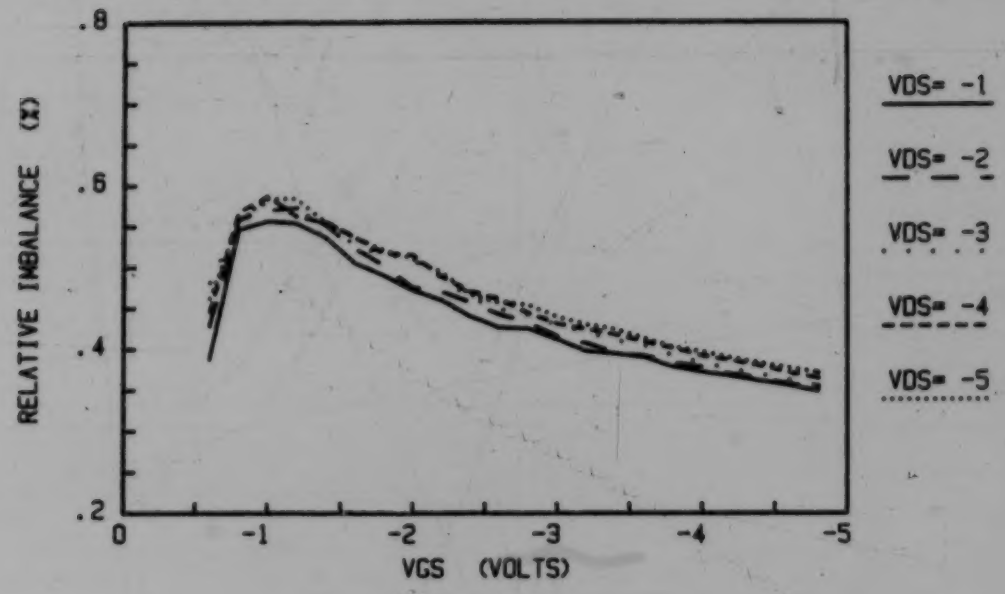

Fig. 4.10 As in Fig. 4.6, but for the PMOS MAGFET (W/L=75μm/25μm).

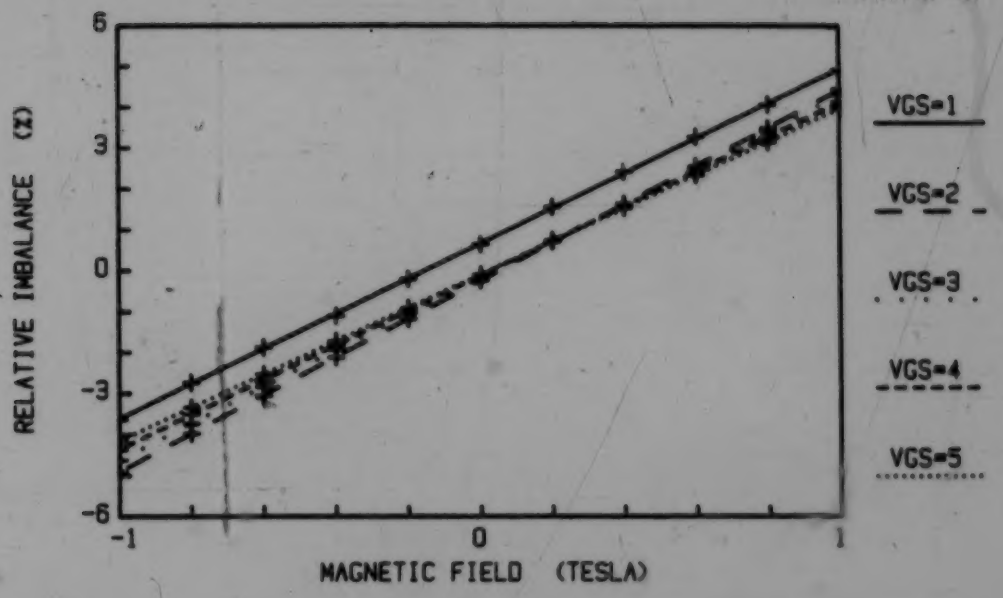

Fig. 4.11 Relative current imbalance (%) as a function of magnetic field at various operating points for the square MAGFET (W/L=100μm/100μm), fabricated via Microtel Pacific. V_{DS}= 5.0 V.

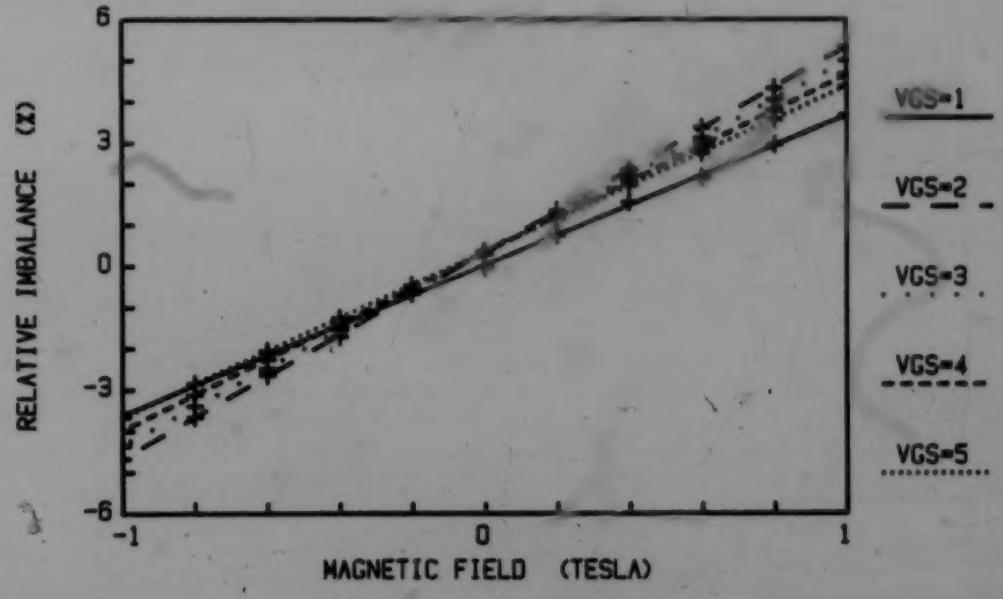

Fig. 4.12 As in Fig. 4.11, but for the square MAGFET (W/L=25μm/25μm).

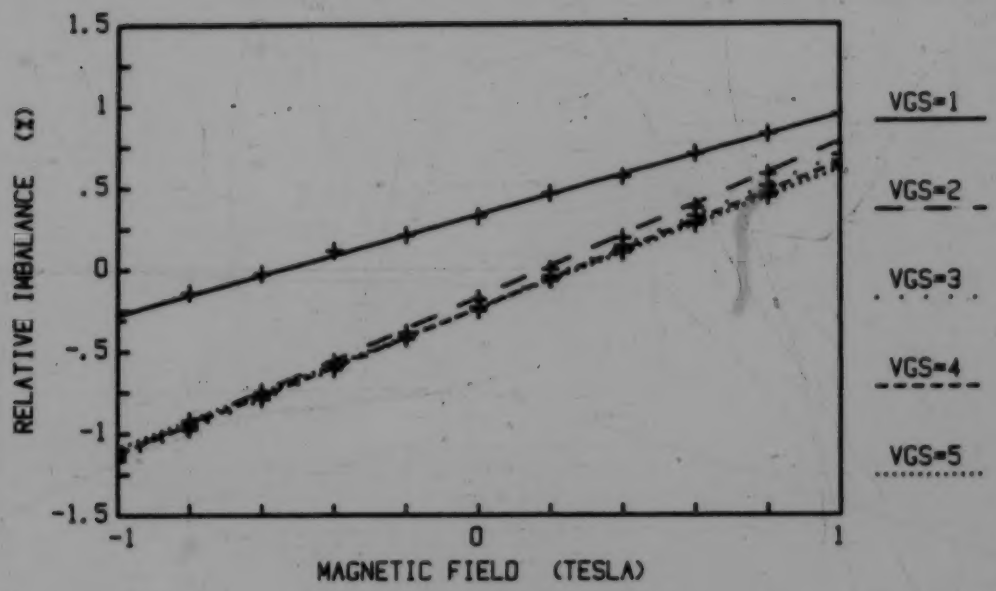

Fig. 4.13 As in Fig. 4.11, but for the wide MAGFET (W/L=100μm/25μm).

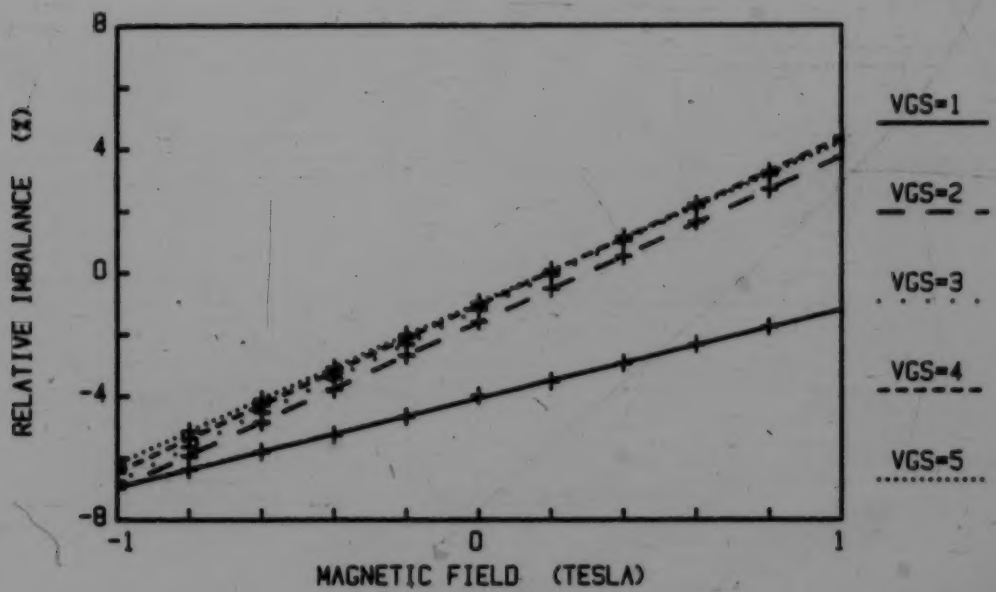

Fig. 4.14 As in Fig. 4.11, but for the long MAGFET (W/L=25μm/100μm).

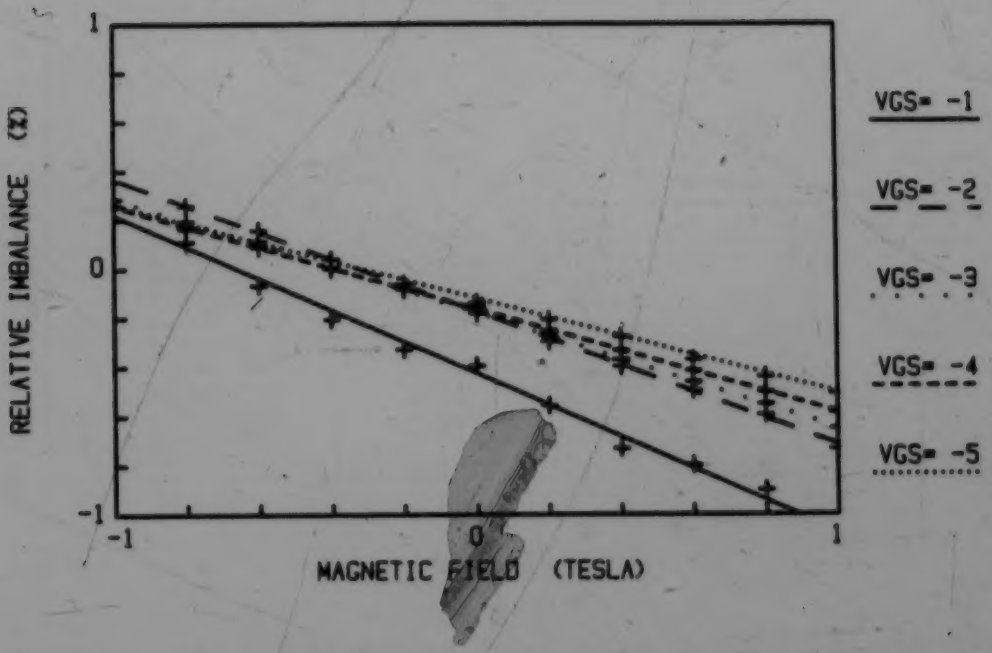

Fig. 4.15 As in Fig. 4.11, but for the PMOS MAGFET (W/L=75μm/25μm). V_{DS}= -5.0 V.

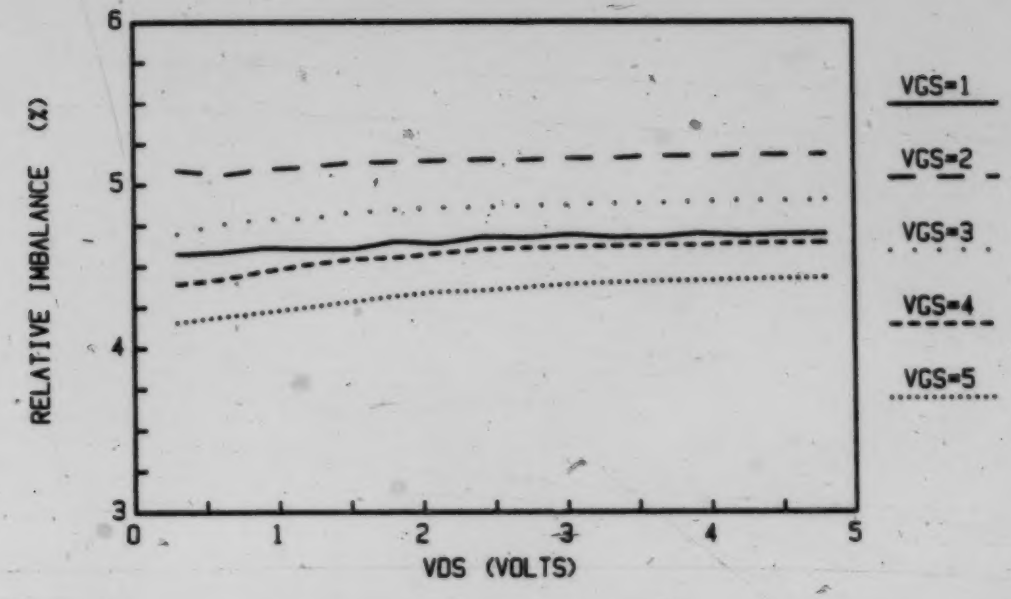

Fig. 4.16 Relative current imbalance at 1 Tesla as a function of operating point for the square MAGFET (W/L=100μm/100μm), fabricated via Northern Telecom.

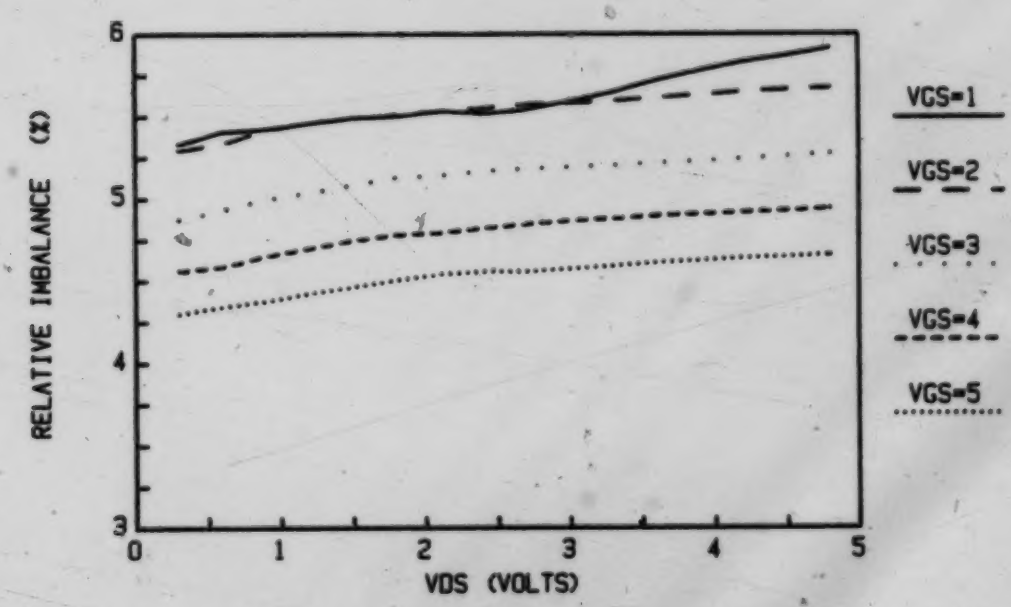

Fig. 4.17 As in Fig. 4.16, but for the square MAGFET (W/L=25μm/25μm).

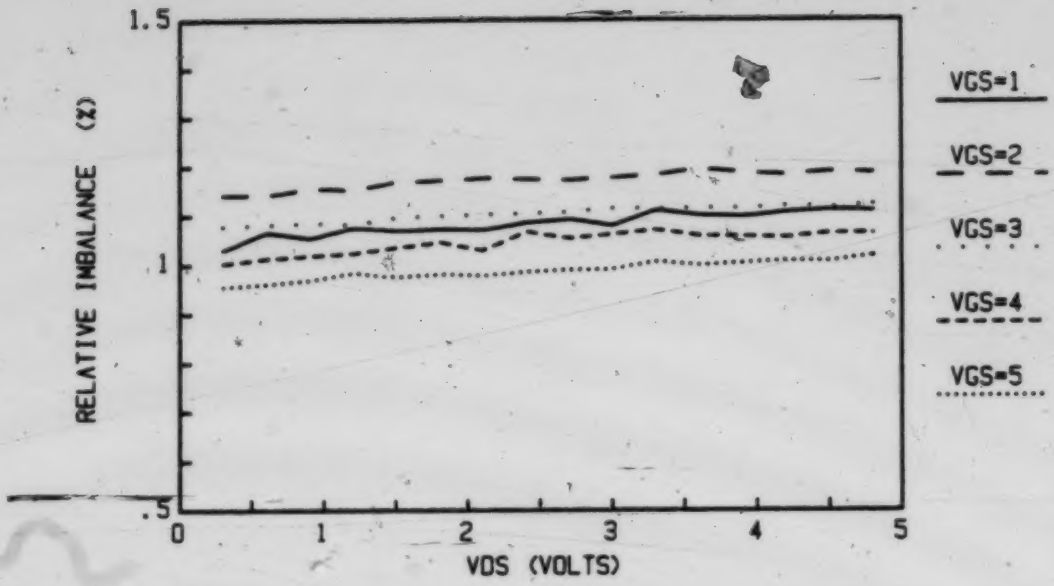

Fig. 4.18 As in Fig. 4.16, but for the wide MAGFET (W/L=100μm/25μm).

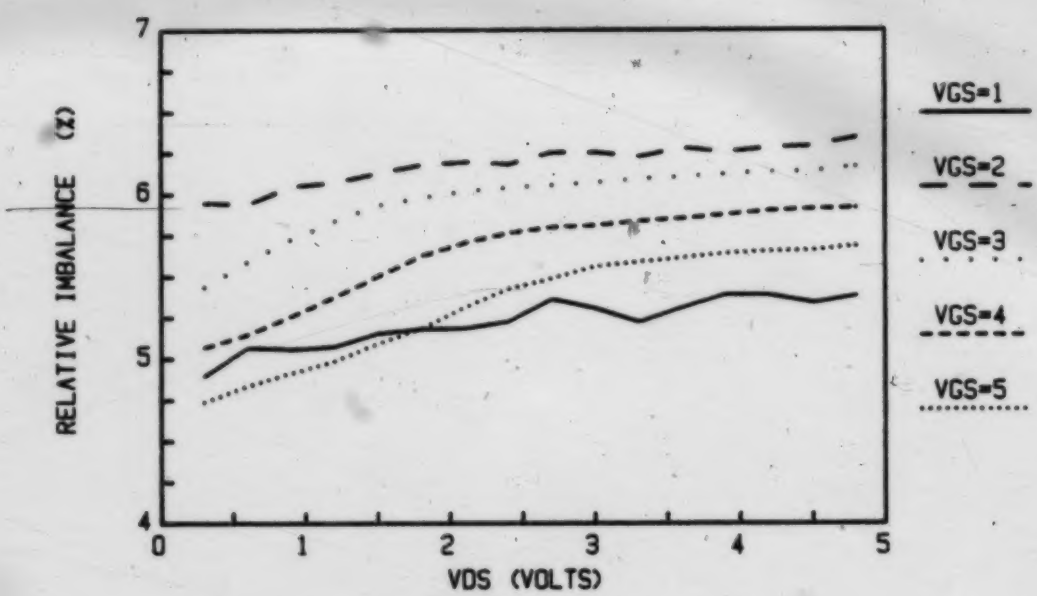

Fig. 4.19 As in Fig. 4.16, but for the long MAGFET (W/L=25μm/100μm).

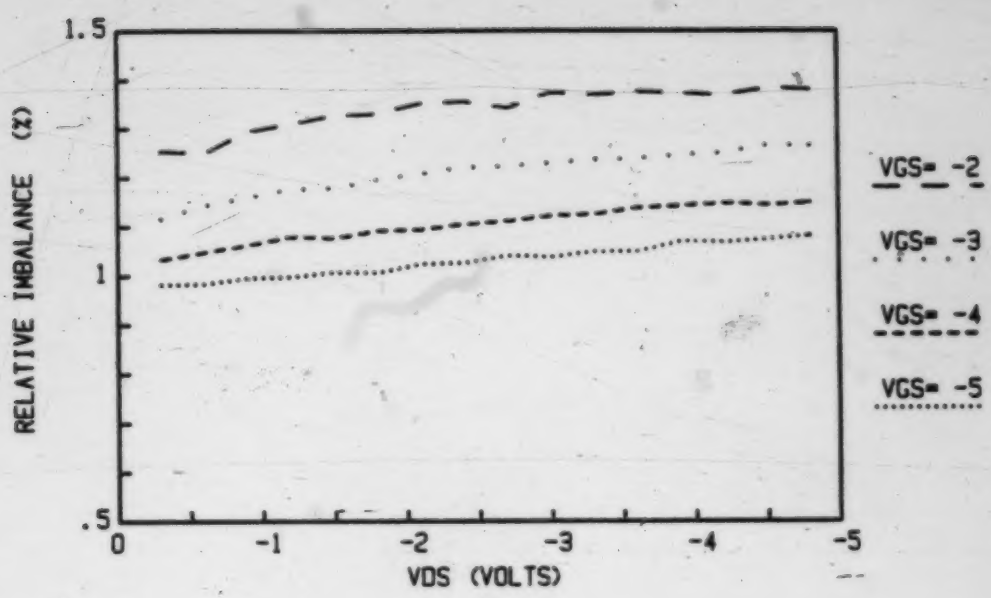

Fig. 4.20 As in Fig. 4.16, but for the PMOS MAGFET (W/L=75μm/25μm).

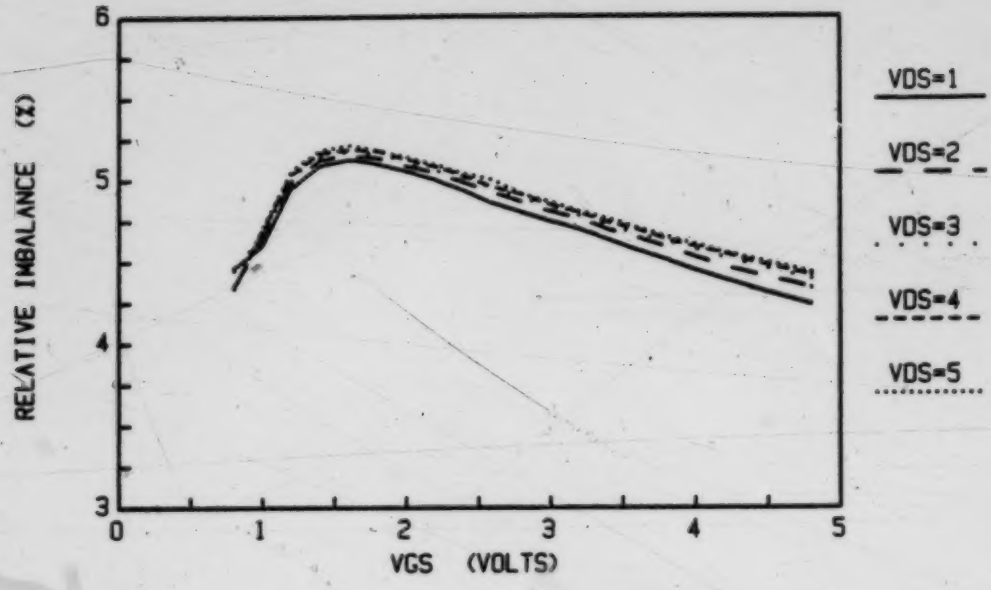

Fig. 4.21 Relative current imbalance at 1 Tesla as a function of operating point for the square MAGFET (W/L=100μm/100μm), fabricated via Northern Telecom.

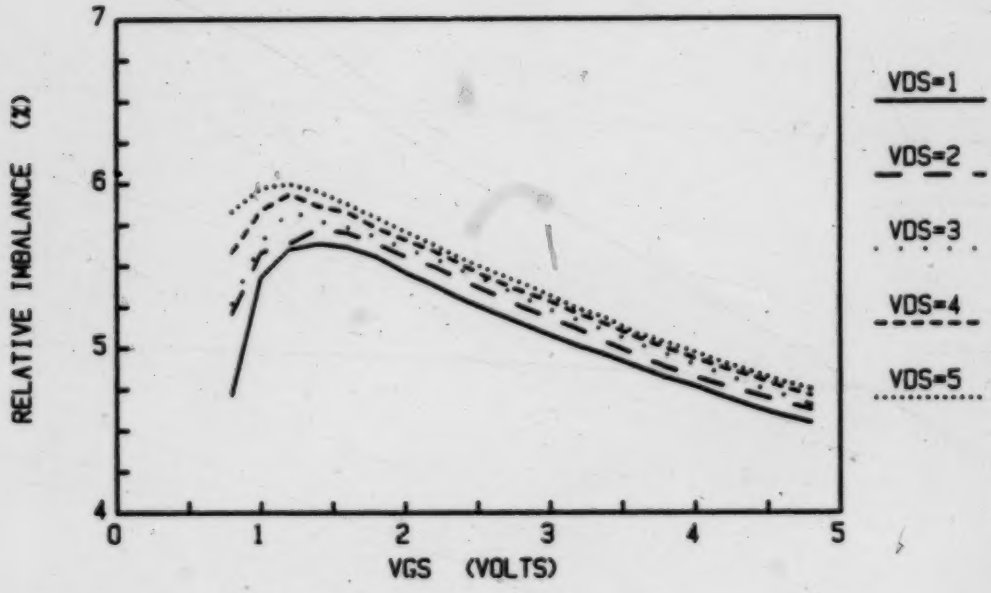

Fig. 4.22 As in Fig. 4.21, but for the square MAGFET (W/L=25μm/25μm).

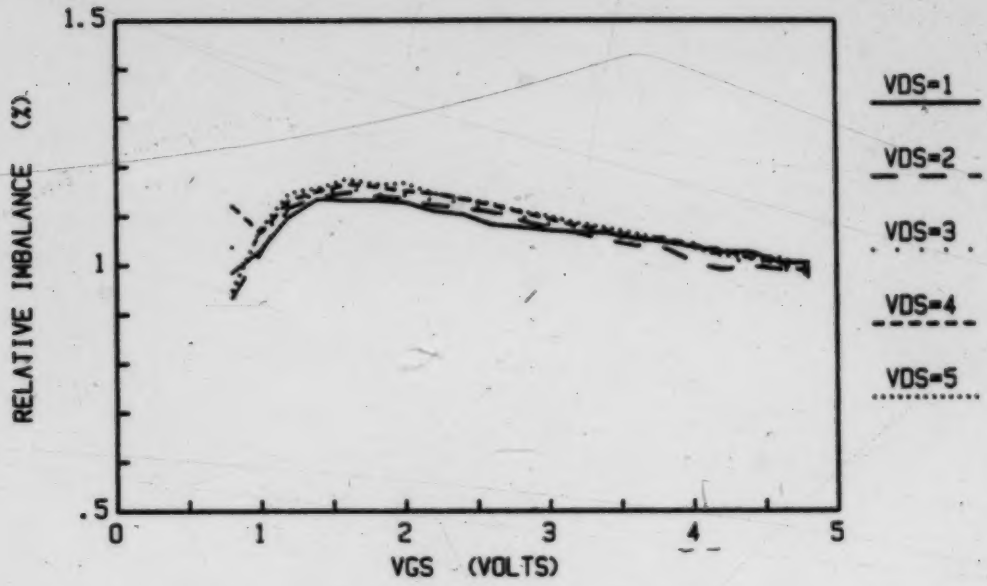

Fig. 4.23 As in Fig. 4.16, but for the wide MAGFET (W/L=100μm/25μm).

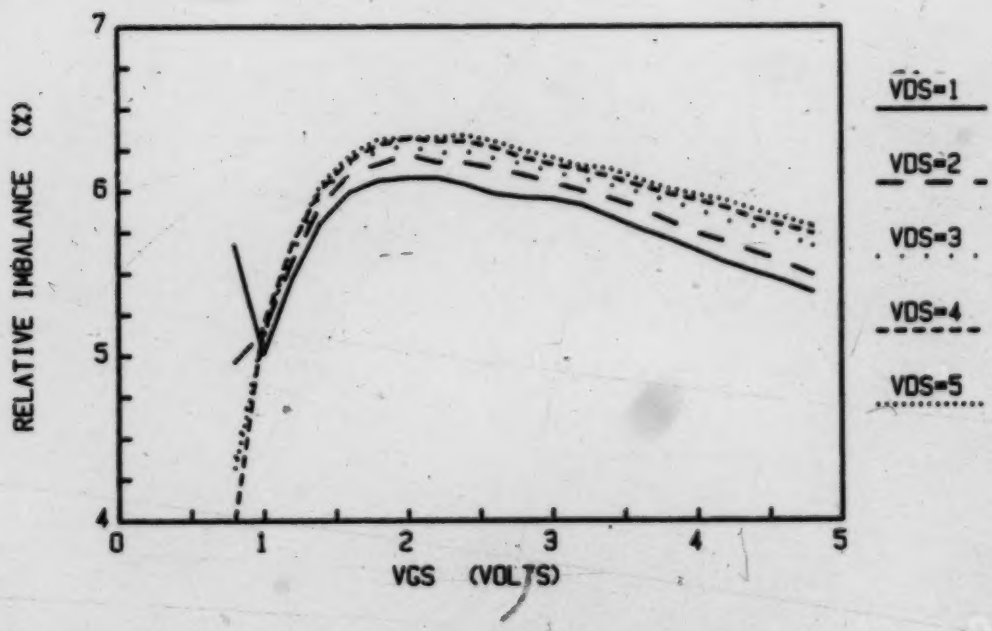

Fig. 4.24 As in Fig. 4.21, but for the long MAGFET (W/L=25μm/100μm).

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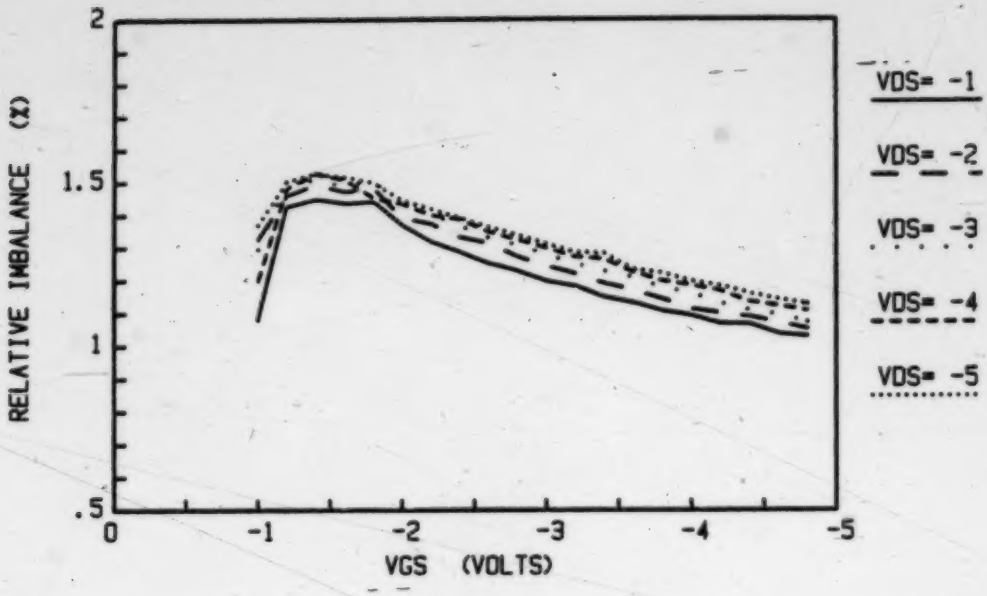

Fig. 4.25 As in Fig. 4.21, but for the PMOS MAGFET (W/L=75μm/25μm).

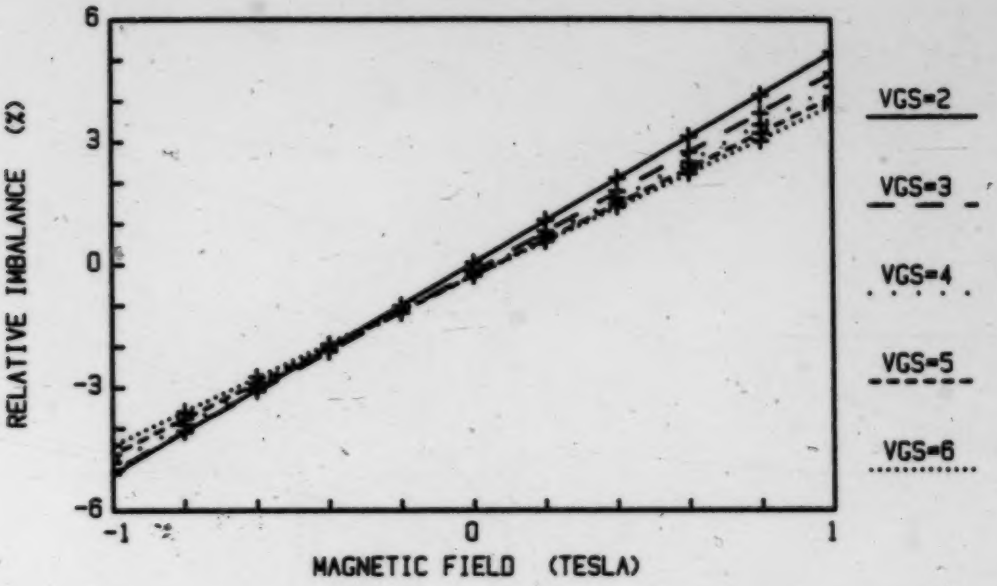

Fig. 4.26 Relative current imbalance as a function of magnetic field at various operating points for the square MAGFET (W/L=100μm/100μm), fabricated via Northern Telecom. V_{DS}= 5.0 V.

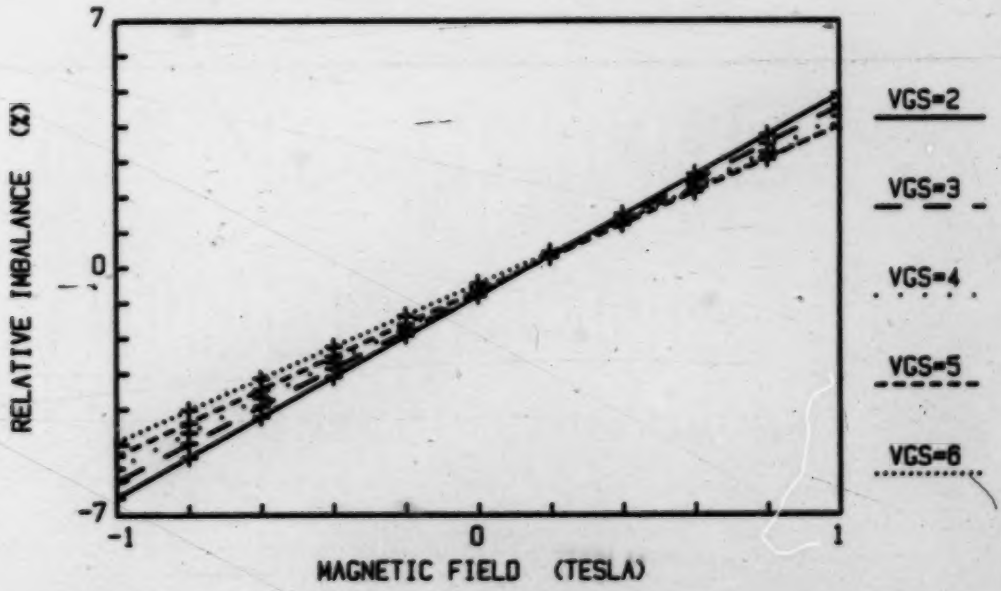

Fig. 4.27 As in Fig. 4.26, but for the square MAGFET (W/L=25μm/25μm).

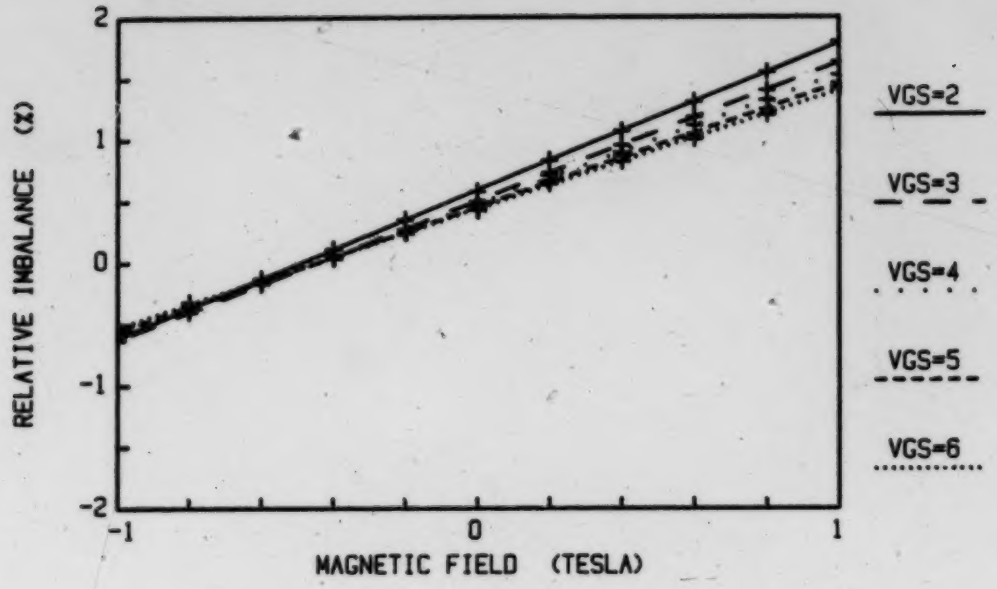

Fig. 4.28 As in Fig. 4.26, but for the wide MAGFET (W/L=100μm/25μm).

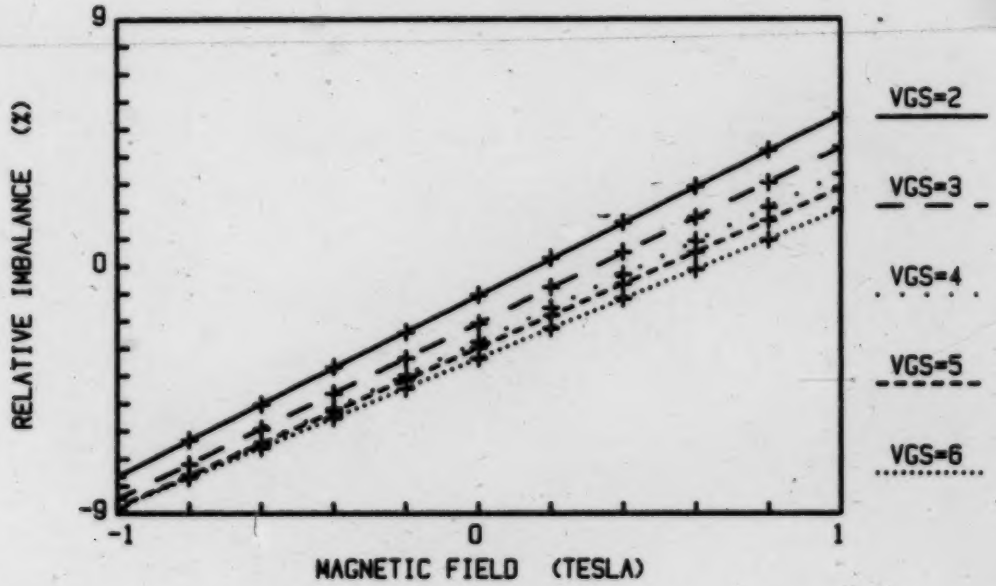

Fig. 4.29 As in Fig. 4.26, but for the long MAGFET (W/L=25μm/100μm).

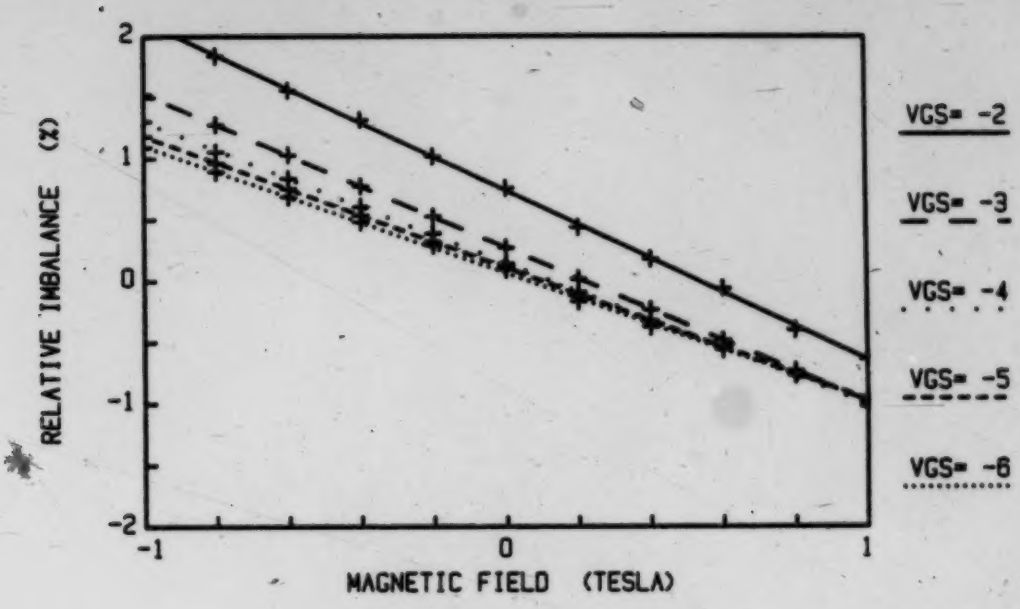

Fig. 4.30 As in Fig. 4.26, but for the PMOS MAGFET (W/L=75μm/25μm). V_{DS}= -5.0 V.

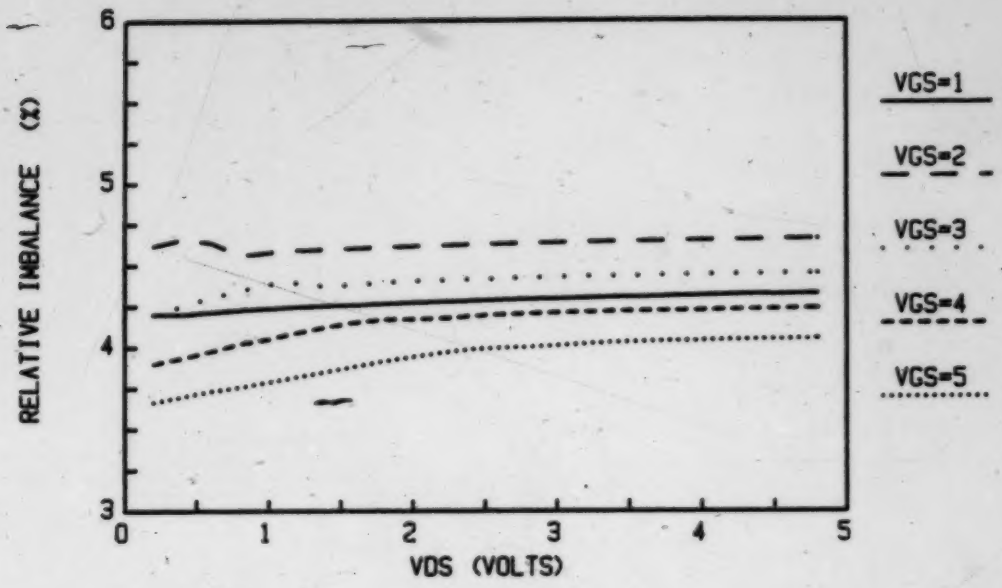

Fig. 4.31 Average relative current imbalance at 1 Tesla as a function of operating point, of nine square MAGFETs (W/L=100μm/100μm), fabricated via Microtel Pacific.

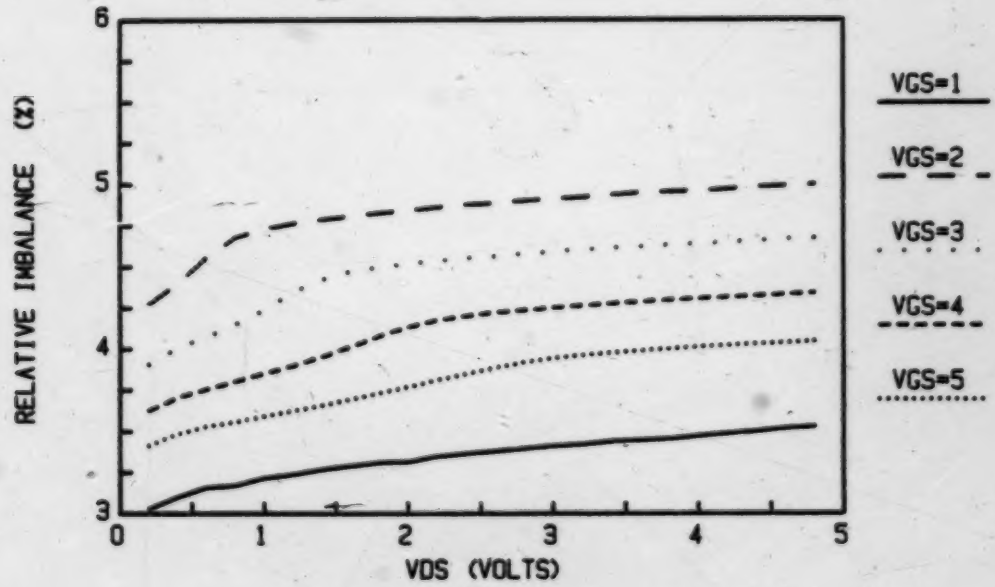

Fig. 4.32 As in Fig. 4.31, but for the square MAGFET (W/L=25μm/25μm).

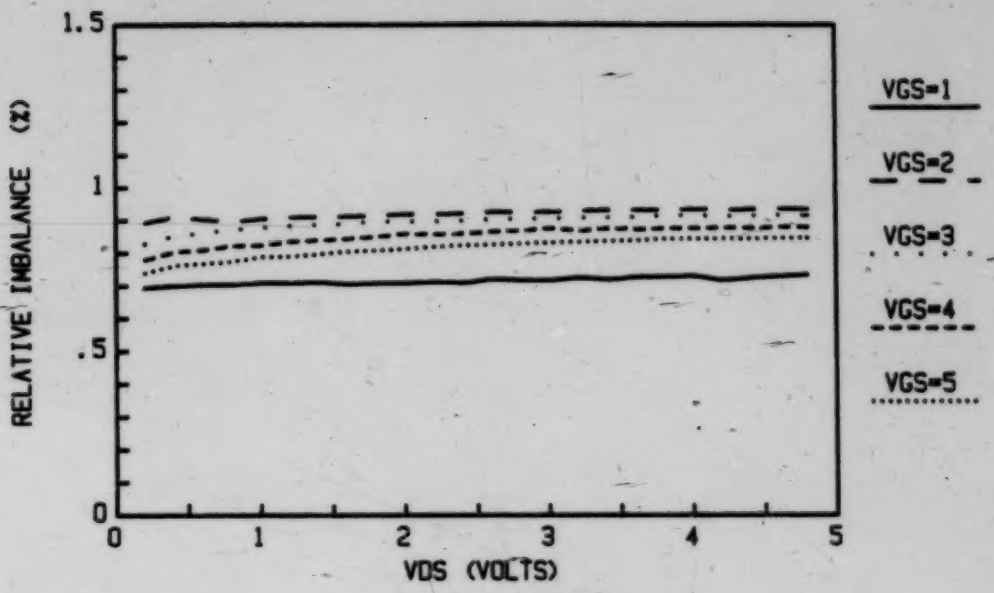

Fig. 4.33 As in Fig. 4.31, but for eight wide MAGFETs (W/L=100μm/100μm).

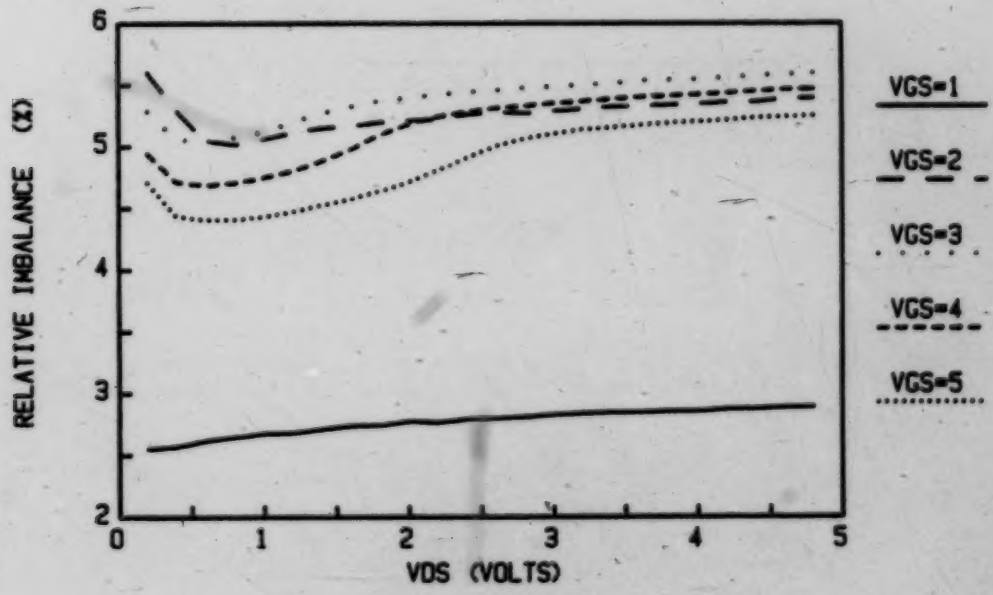

Fig. 4.34 As in Fig. 4.31, but for six long MAGFETs (W/L=25μm/100μm).

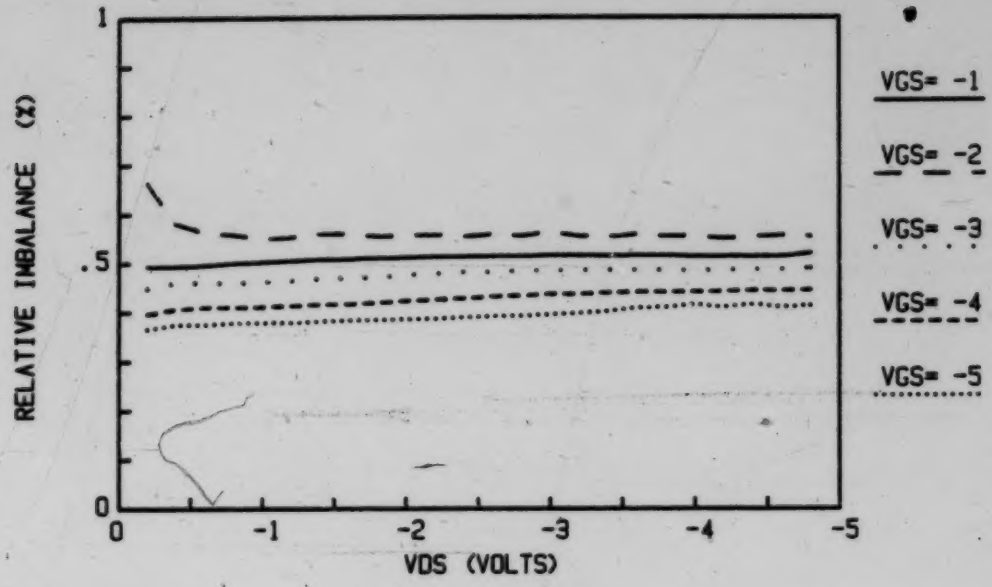

Fig. 4.35 As in Fig. 4.31, but for seven PMOS MAGFETs (W/L=75μm/25μm).

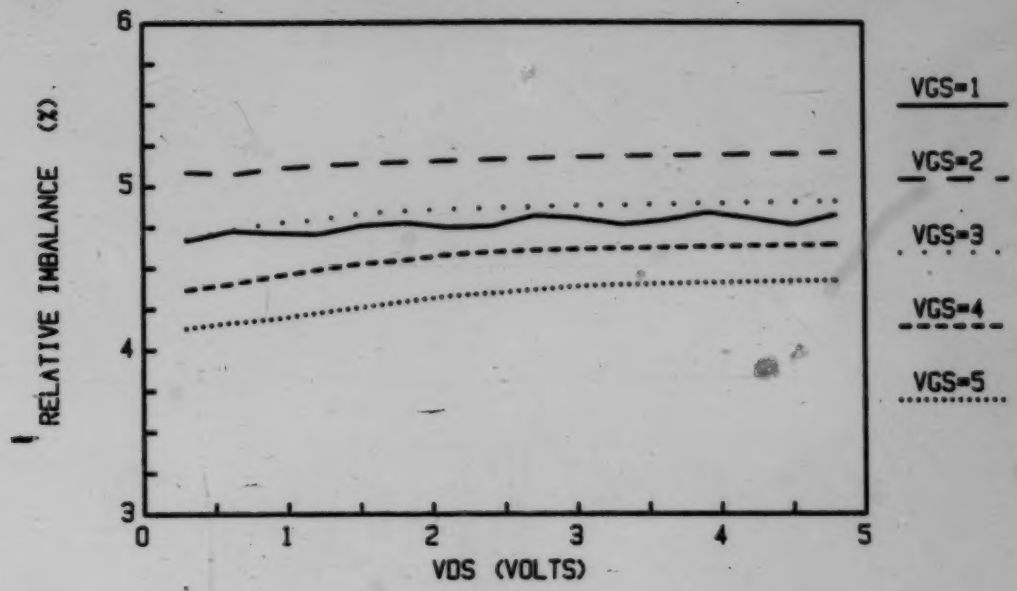

Fig. 4.36 Average relative current imbalance at 1 Tesla as a function of operating point, of ten square MAGFETs (W/L=100μm/100μm), fabricated via Northern Telecom.

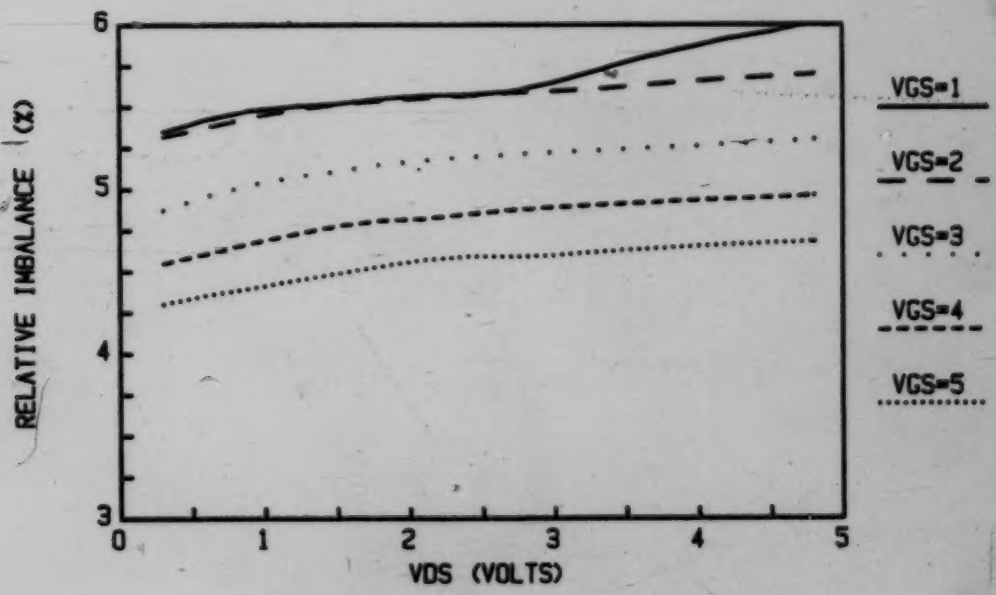

Fig. 4.37 As in Fig. 4.36, but for the square MAGFET (W/L=25μm/25μm).

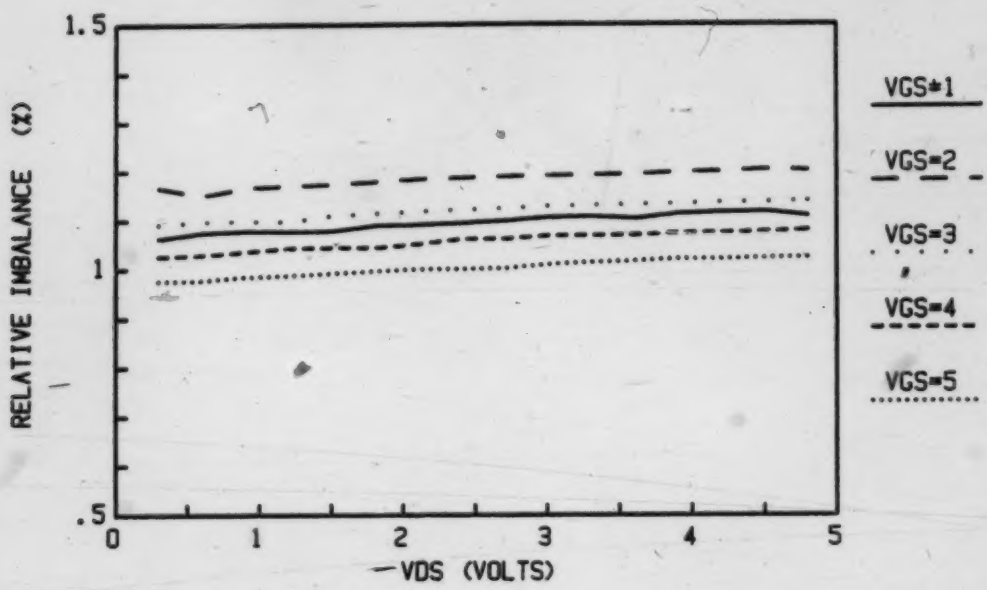

Fig. 4.38 As in Fig. 4.36, but for the wide MAGFET (W/L=100μm/25μm).

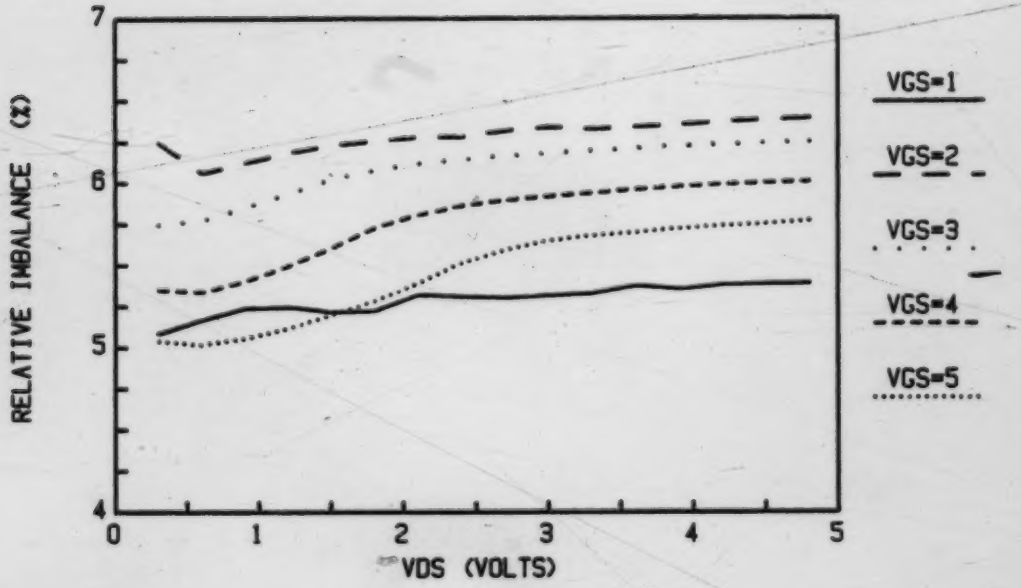

Fig. 4.39 As in Fig. 4.36, but for the long MAGFET (W/L=25μm/100μm).

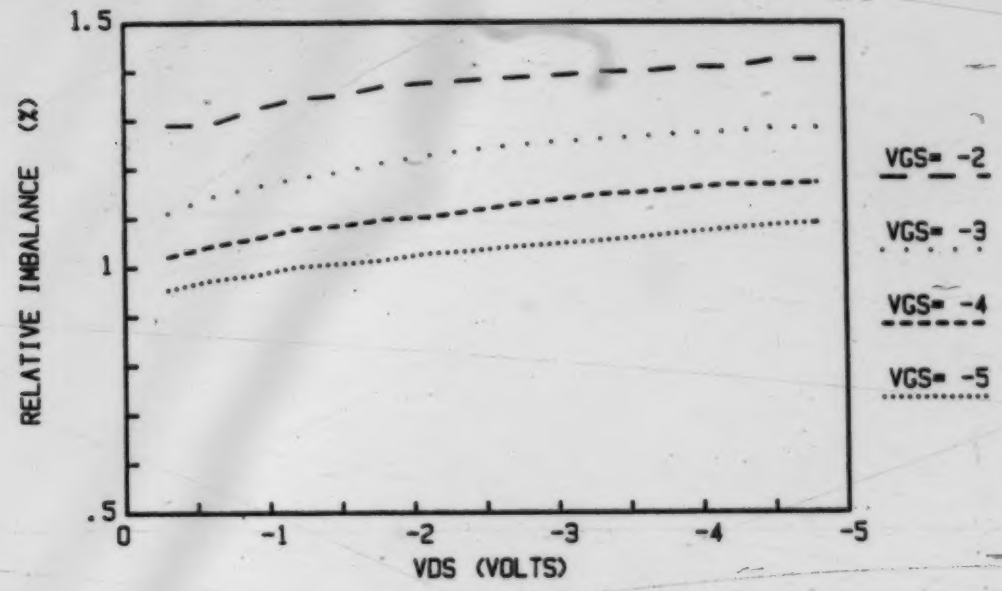

Fig. 4.40 As in Fig. 4.36, but for the PMOS MAGFET (W/L=75μm/25μm).

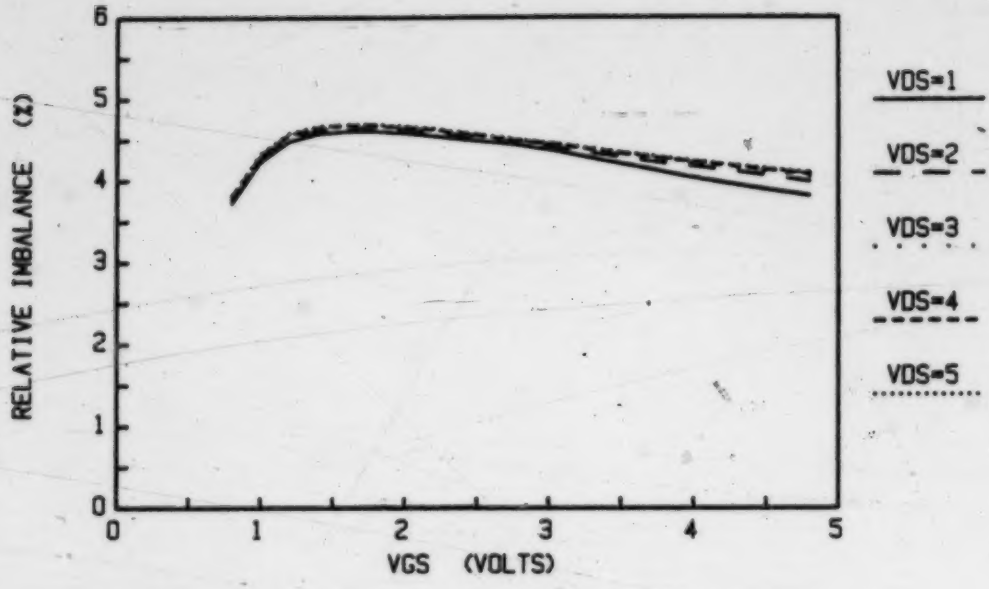

Fig. 4.41 Average relative current imbalance at 1 Tesla as a function of operating point, of six square MAGFETs (W/L=100μm/100μm), fabricated via Microtel Pacific.

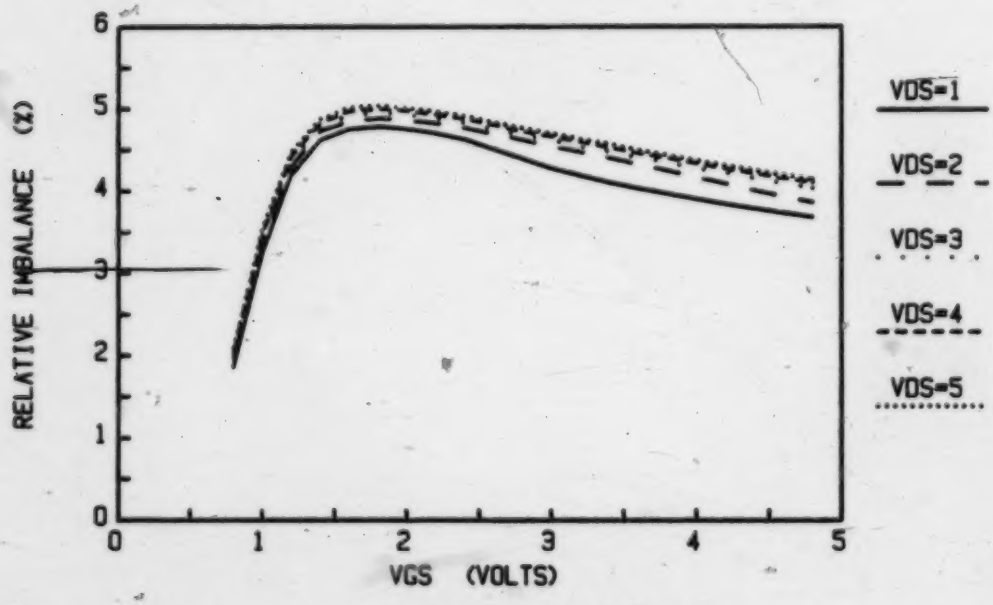

Fig. 4.42 As in Fig. 4.41, but for five square MAGFETs (W/L=25μm/25μm).

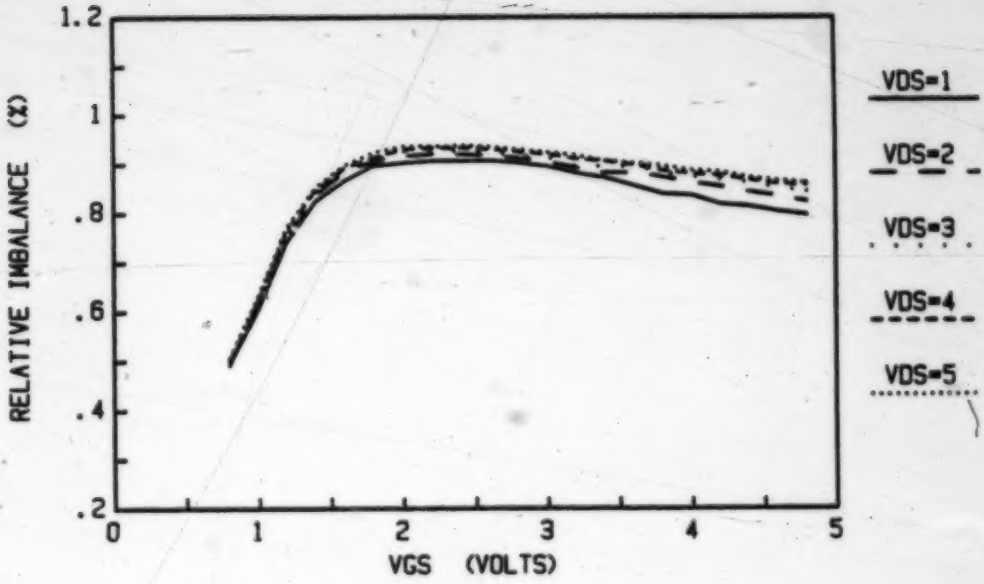

Fig. 4.43 As in Fig. 4.41, but for five wide MAGFETs (W/L=100μm/25μm).

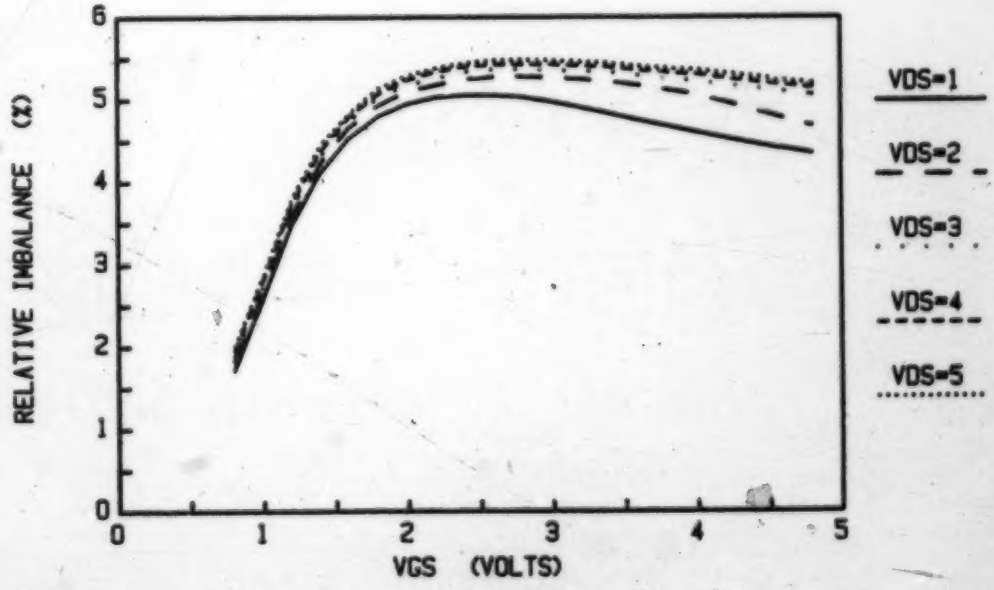

Fig. 4.44 As in Fig. 4.41, but for five long MAGFETs (W/L=25μm/100μm).

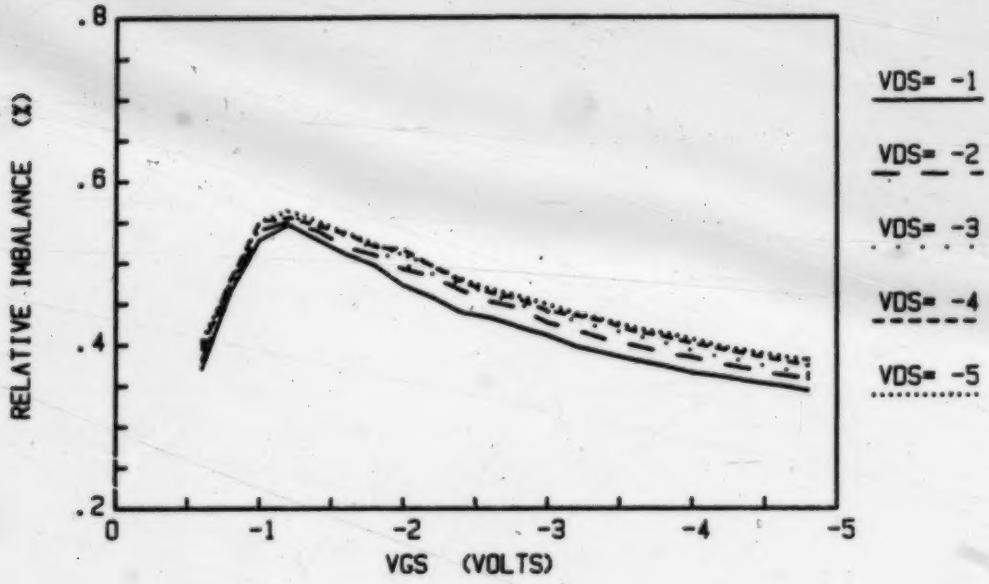

Fig. 4.45 As in Fig. 4.41, but for three PMOS MAGFETs (W/L=75μm/25μm).

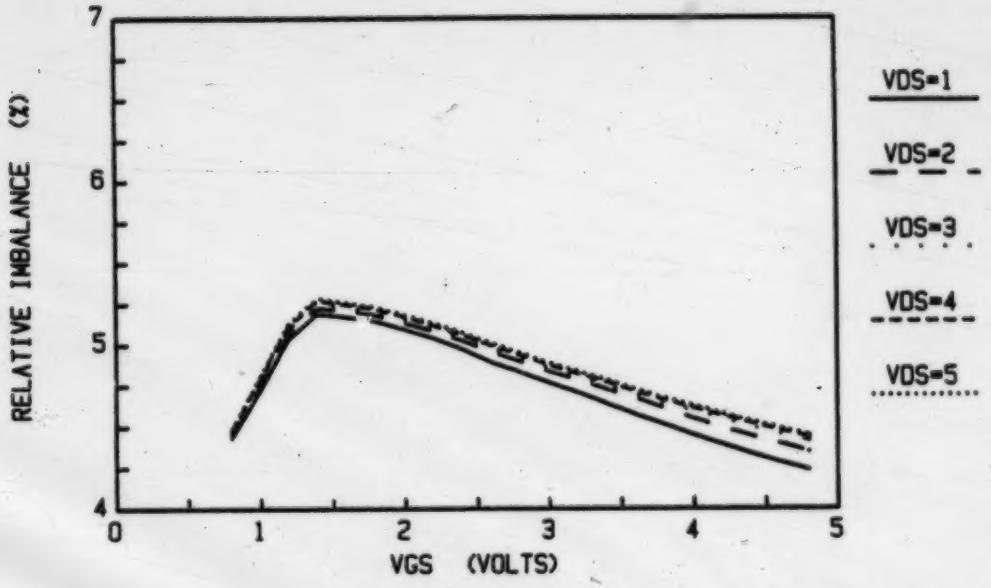

Fig. 4.46 Average relative current imbalance at 1 Tesla as a function of operating point, of ten square MAGFETs (W/L=100μm/100μm), fabricated via Northern Telecom.

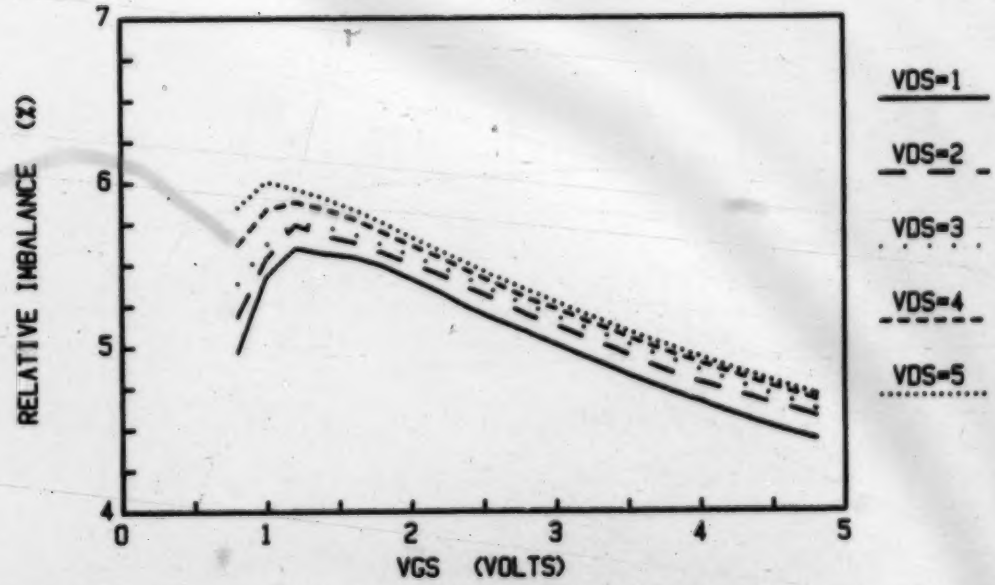

Fig. 4.47 As in Fig. 4.46, but for the square MAGFET (W/L=25μm/25μm).

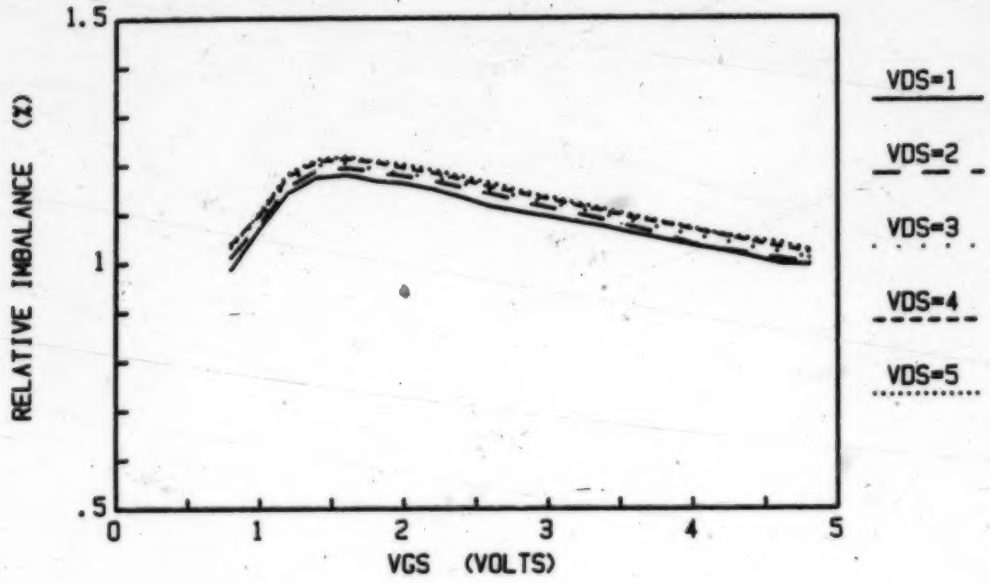

Fig. 4.48 As in Fig. 4.46, but for the wide MAGFET (W/L=100μm/25μm).

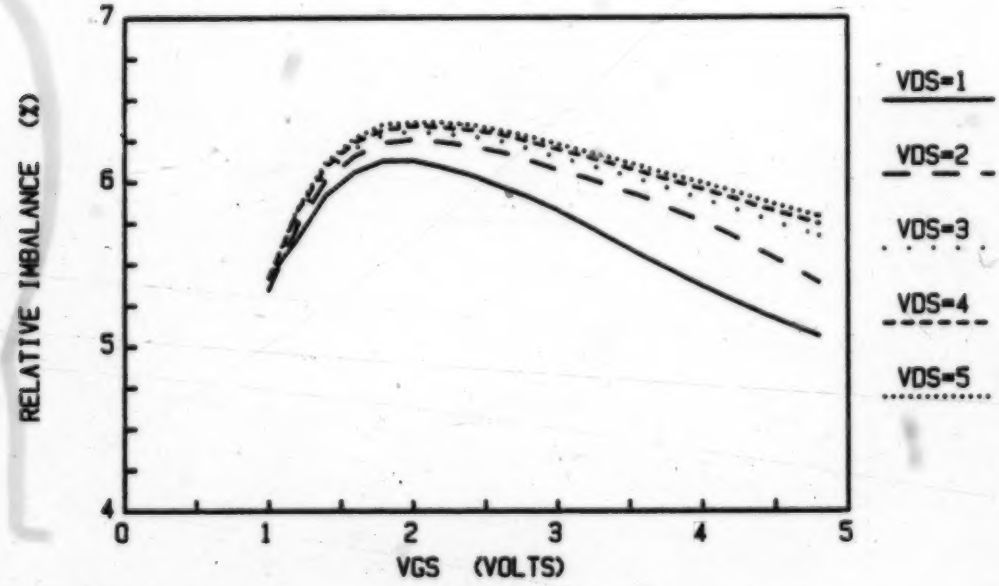

Fig. 4.49 As in Fig. 4.46, but for the long MAGFET (W/L=25μm/100μm).

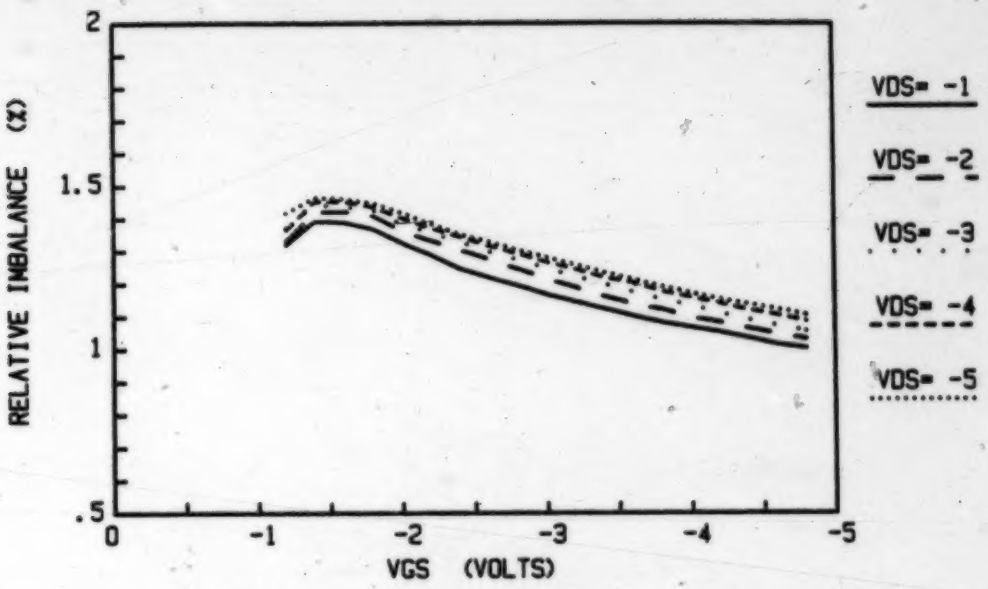

Fig. 4.50 As in Fig. 4.46, but for the PMOS MAGFET (W/L=75μm/25μm).

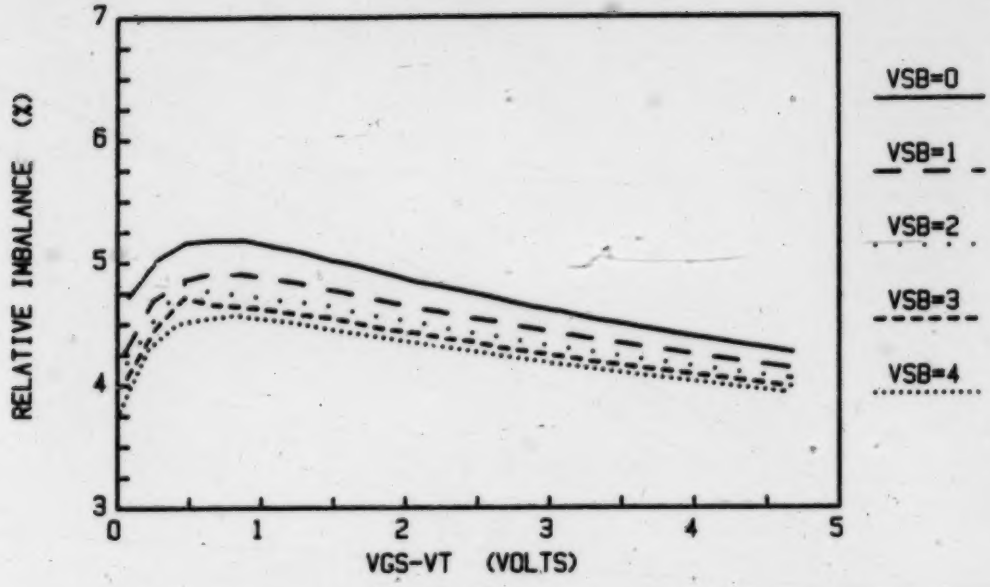

Fig. 4.51 Average relative current imbalance at 1 Tesla as a function of $(V_{GS}-V_T)$ for various values of V_{SB} with V_{DS}=5 V, of the square MAGFET (W/L=100μm/100μm), fabricated via Northern Telecom.

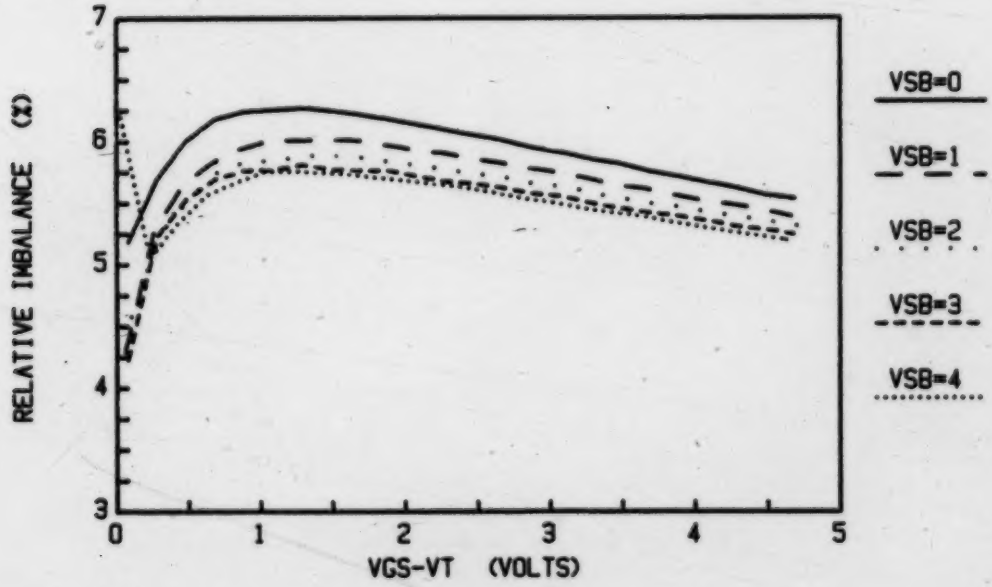

Fig. 4.52 As in Fig. 4.51, but for the long MAGFET (W/L=25μm/100μm).

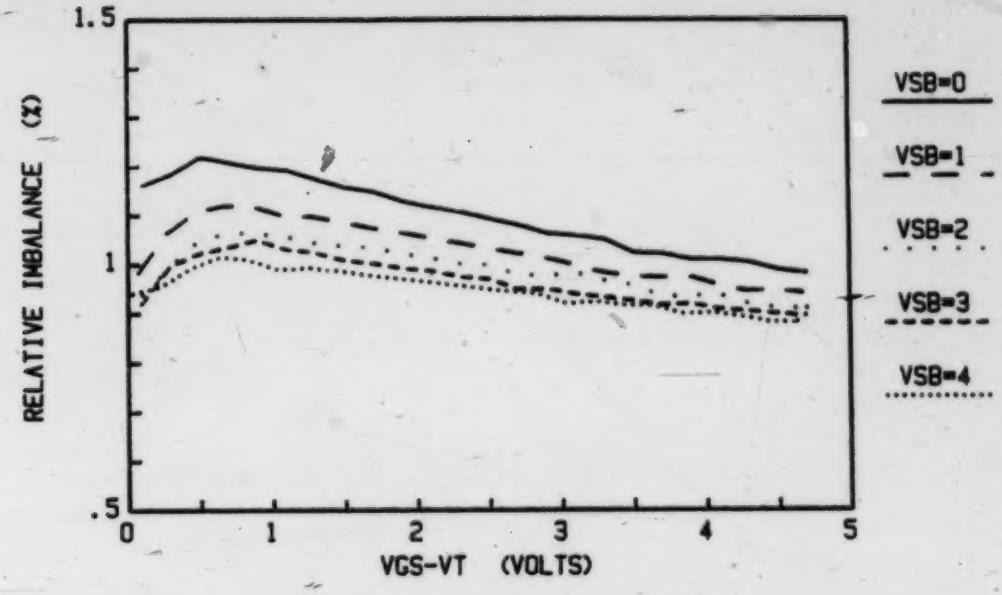

Fig. 4.53 As in Fig. 4.51, but for the wide MAGFET (W/L=100μm/25μm).

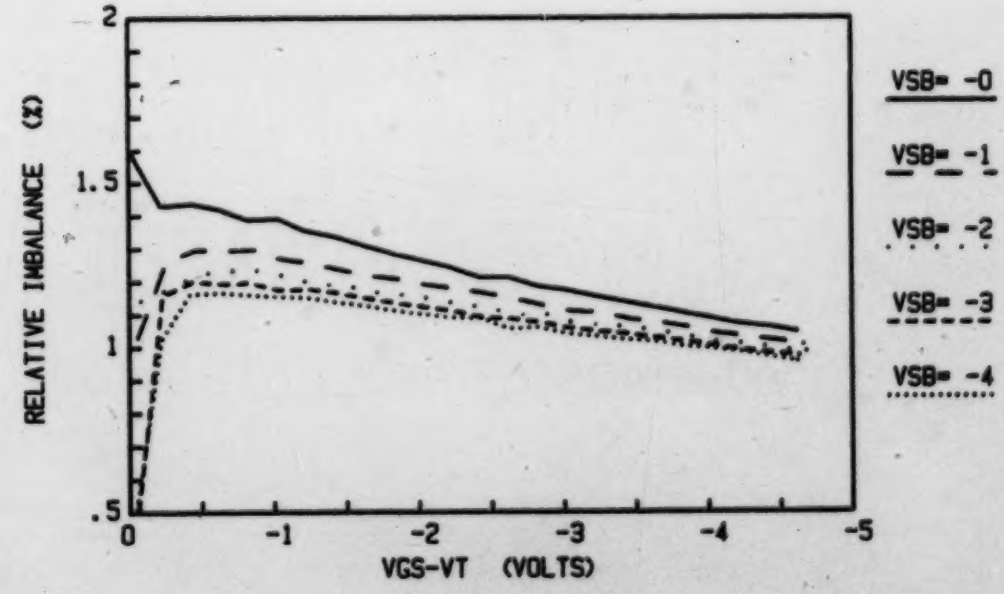

Fig. 4.54 As in Fig. 4.51, but with V_{DS}=-5 V for the PMOS MAGFET (W/L=75μm/25μm).

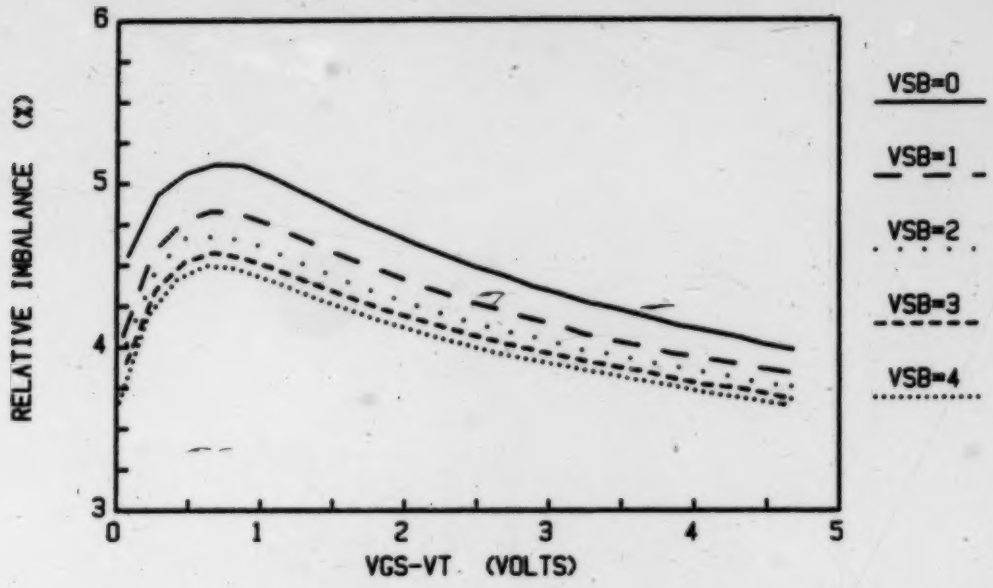

Fig. 4.55 Average relative current imbalance at 1 Tesla as a function of $(V_{GS}-V_T)$ for various values of V_{SB} with V_{DS}=.3 V, of the square MAGAFET (W/L=100μm/100μm), fabricated via Northern Telecom.

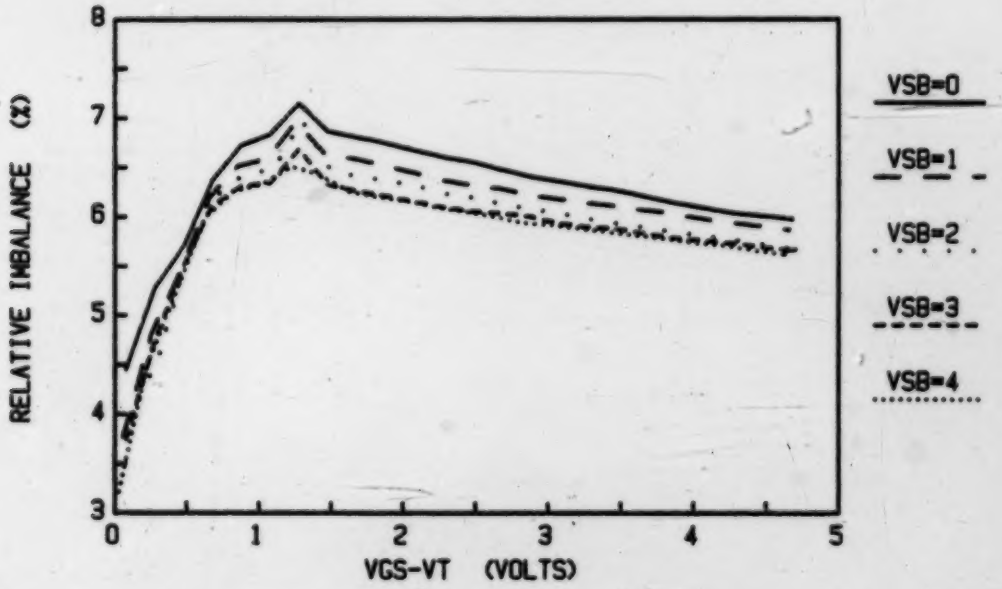

Fig. 4.56 As in Fig. 4.55, but for the long MAGFET (W/L=25μm/100μm).

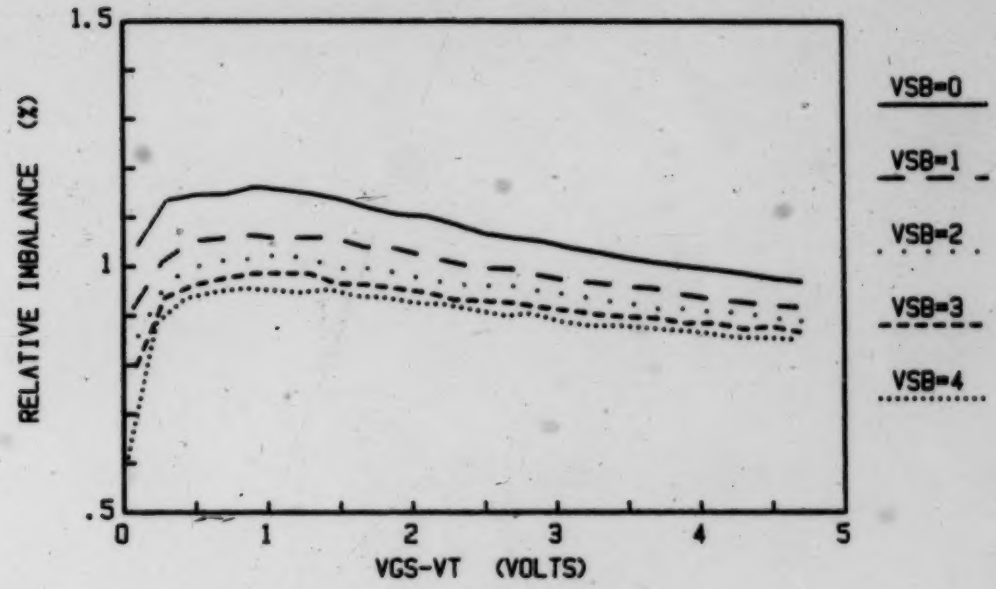

Fig. 4.57 As in Fig. 4.55, but for the wide MAGFET (W/L=100μm/25μm).

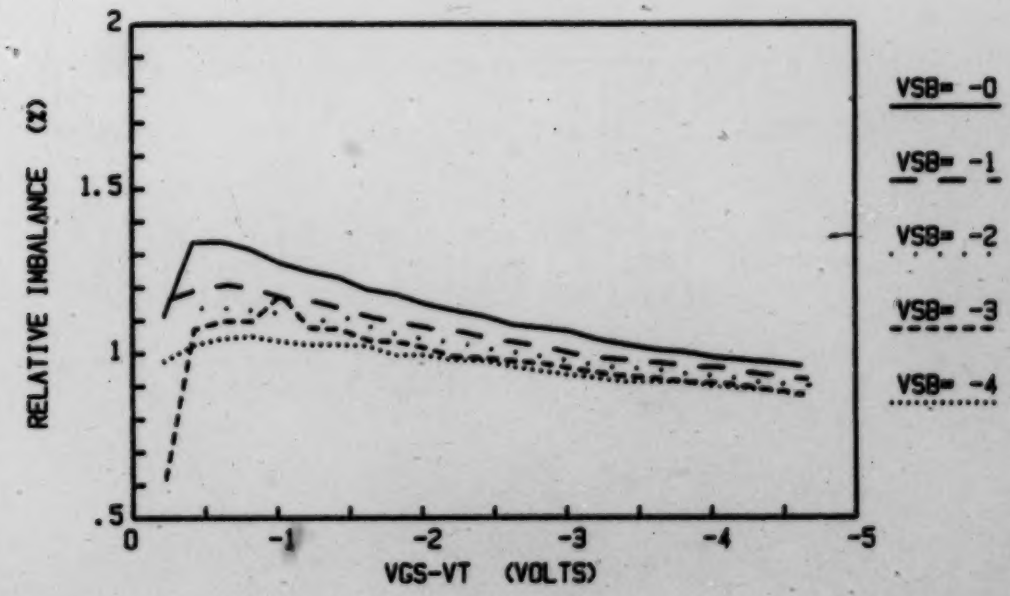

Fig. 4.58 As in Fig. 4.55, but with V_{DS}=-.3 V for the PMOS MAGFET (W/L=75μm/25μm).

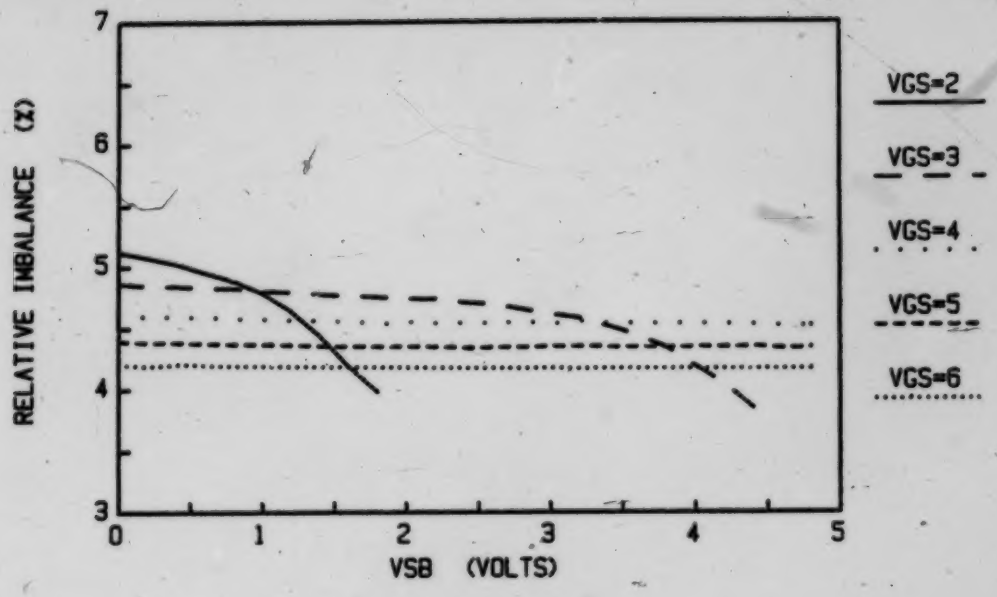

Fig. 4.59 Relative current imbalance at 1 Tesla as a function of V_{SB} for various values of V_{GS} with V_{DS}= 5 V, of the square MAGFET (W/L=100μm/100μm), fabricated via Northern Telecom.

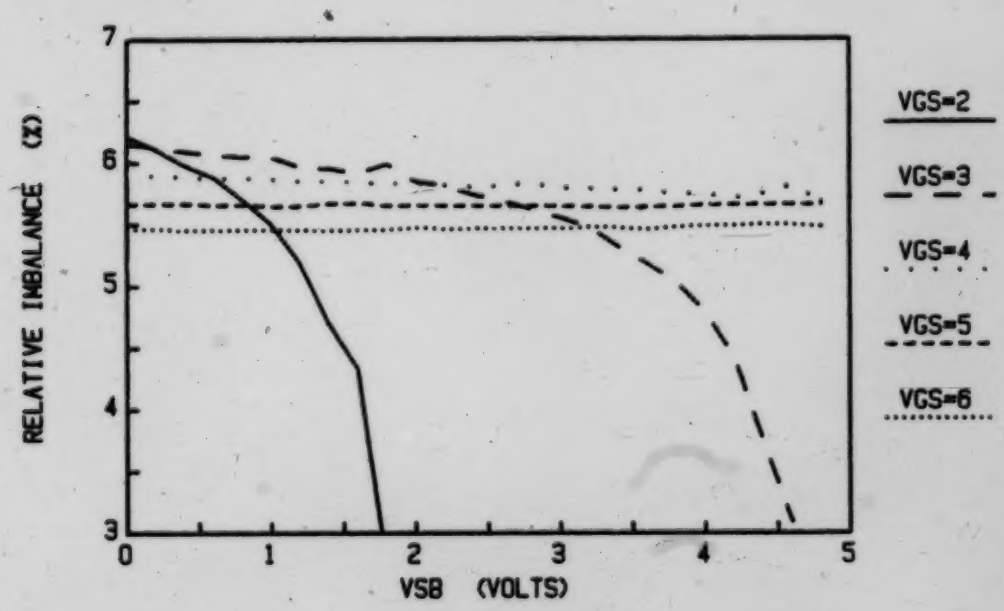

Fig. 4.60 As in Fig. 4.59, but for the long MAGFET (W/L=25μm/100μm).

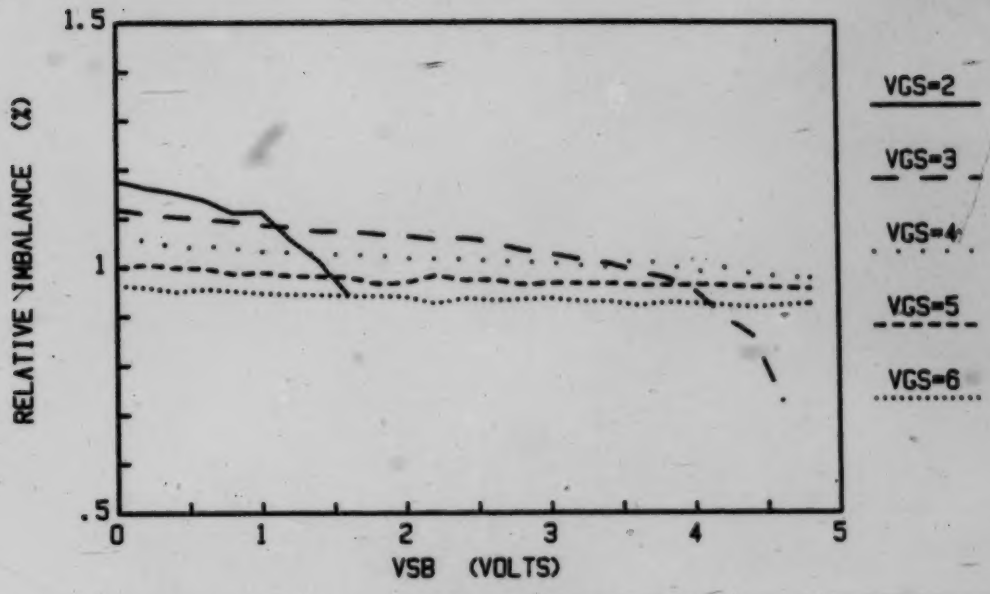

Fig. 4.61 As in Fig. 4.59, but for the wide MAGFET (W/L=100μm/25μm).

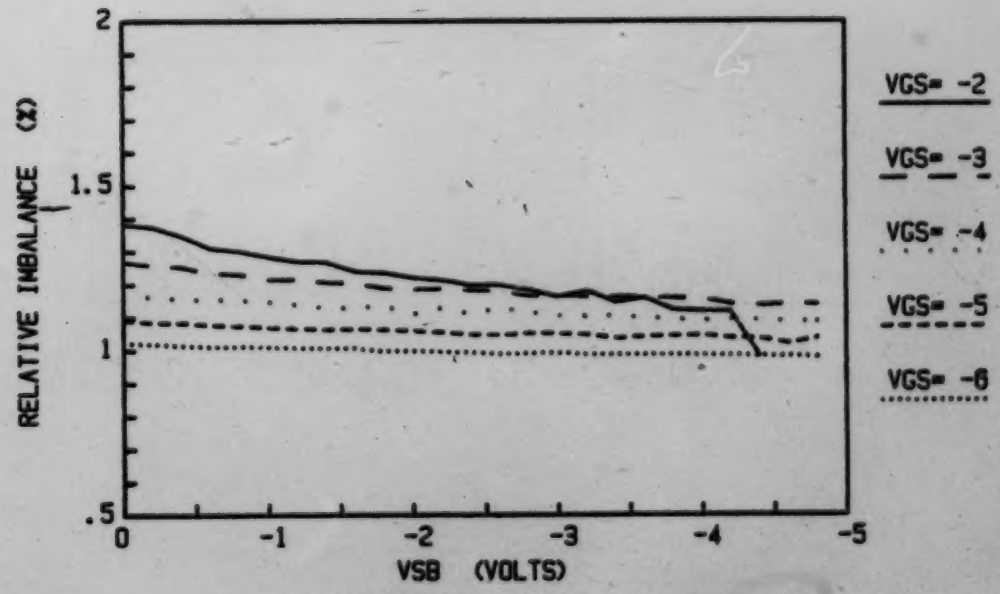

Fig. 4.62 As in Fig. 4.59, but with V_{DS}=-5 V for the PMOS MAGFET (W/L=75μm/25μm).

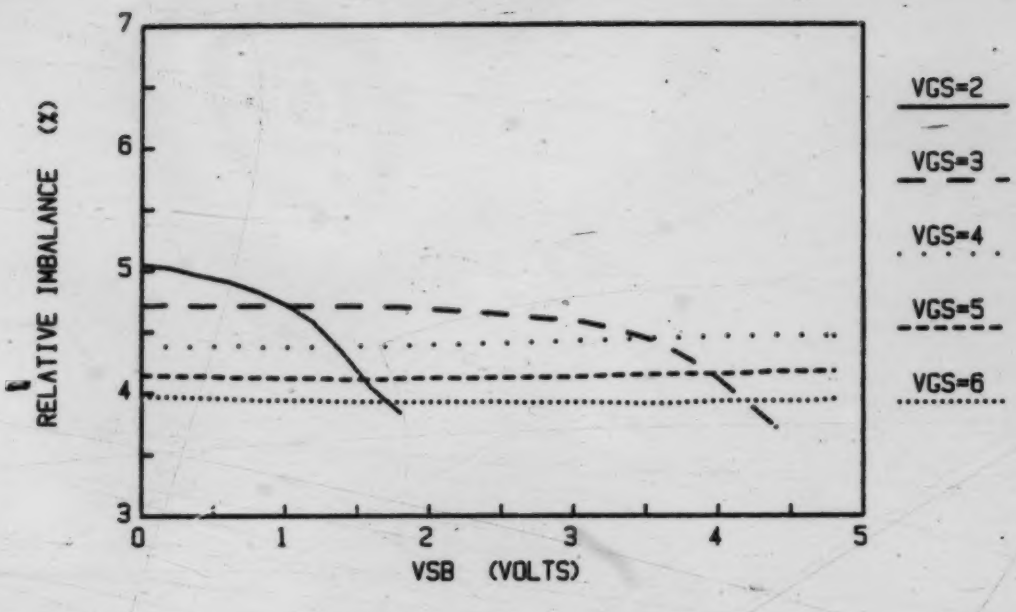

Fig. 4.63 Relative current imbalance at 1 Tesla as a function of V_{SB} for various values of V_{GS} with V_{DS}= .3 V, of the square MAGFET (W/L=100μm/100μm), fabricated via Northern Telecom.

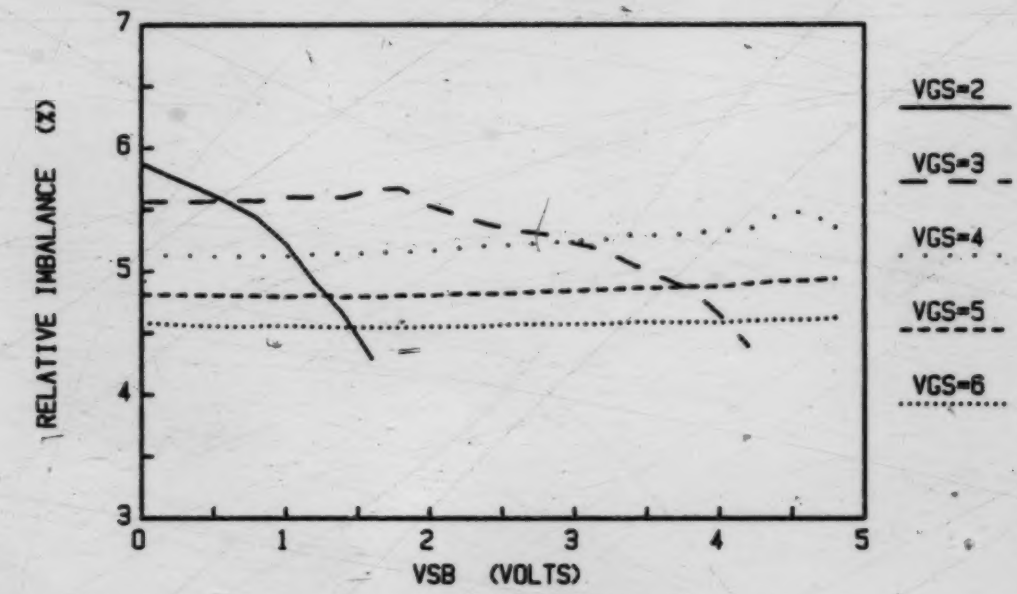

Fig. 4.64 As in Fig. 4.63, but for the long MAGFET (W/L=25μm/100μm).

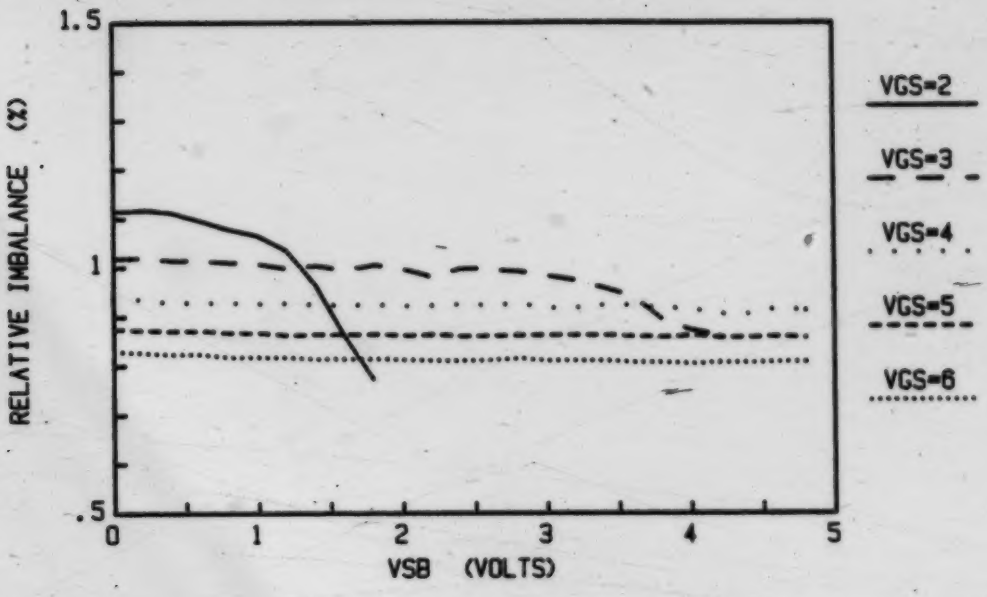

Fig. 4.65 As in Fig. 4.63, but for the wide MAGFET (W/L=100μm/25μm).

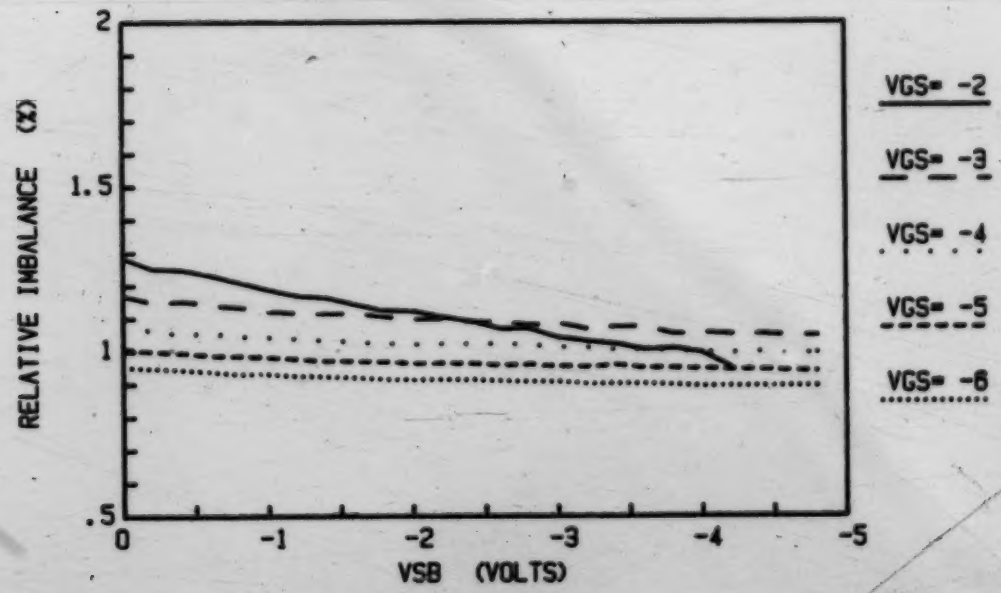

Fig. 4.66 As in Fig. 4.63, but with V_{DS}=-.3 V for the PMOS MAGFET (W/L=75μm/25μm).

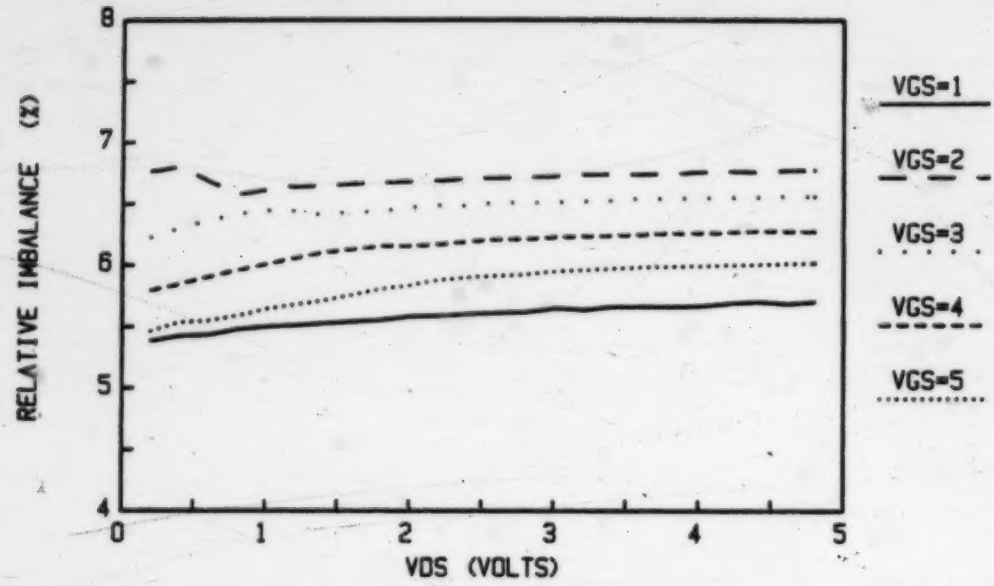

Fig. 4.67 Relative current imbalance (%) as a function of operating point of the triple drain MAGFET, fabricated via Microtel Pacific. Using $\delta = (I_1-I_2)/(I_1+I_2)$.

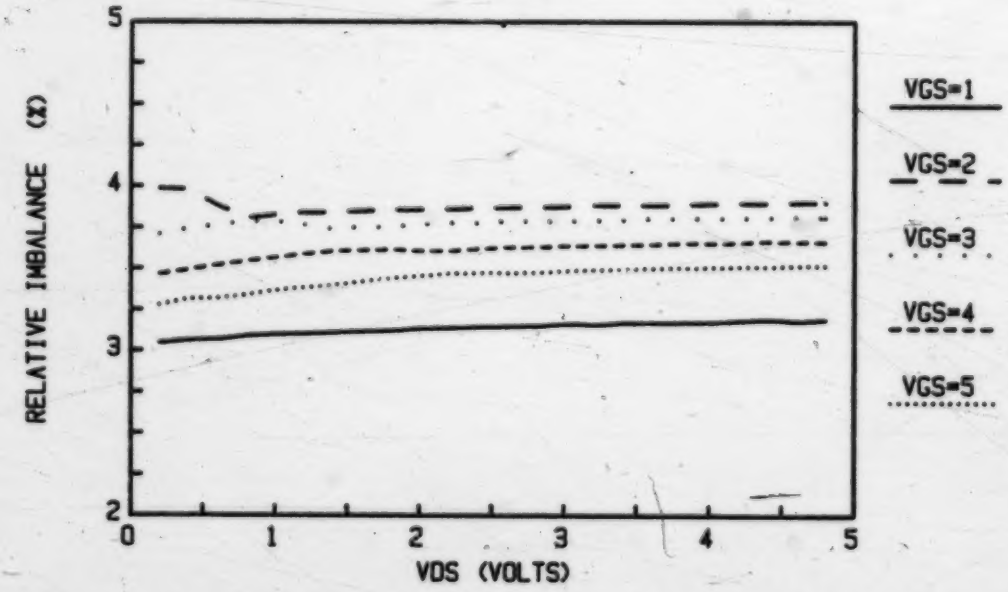

Fig. 4.68 Relative current imbalance (%) as a function of operating point of the triple drain MAGFET, fabricated via Microtel Pacific. Using $\delta = (I_1-I_2)/(I_1+I_2+I_3)$.

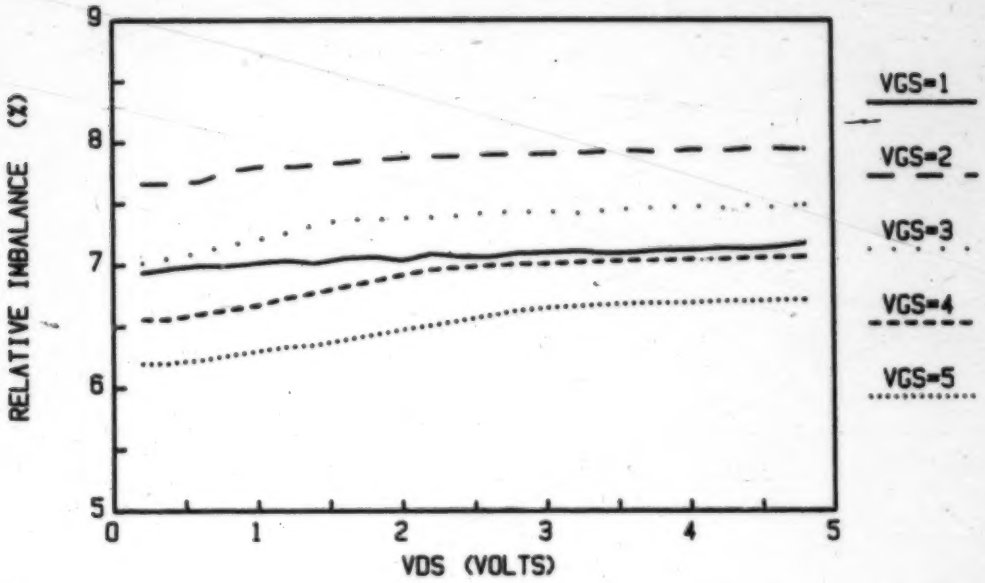

Fig. 4.69 Relative current imbalance (%) as a function of operating point of the triple drain MAGFET, fabricated via Northern Telecom. Using $\delta = (I_1 - I_2)/(I_1 + I_2)$.

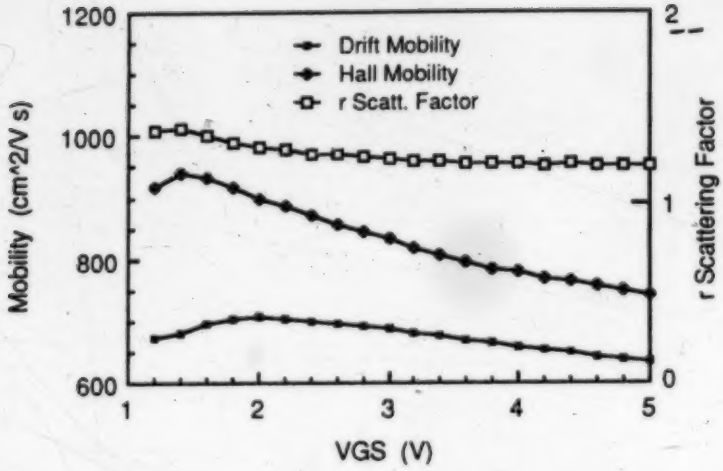

Fig. 4.70 Hall mobility, drift mobility, and scattering factor as a function of V_{GS}. The device is a square MAGFET, (W/L=100μm/100μm), fabricated via Northern Telecom.

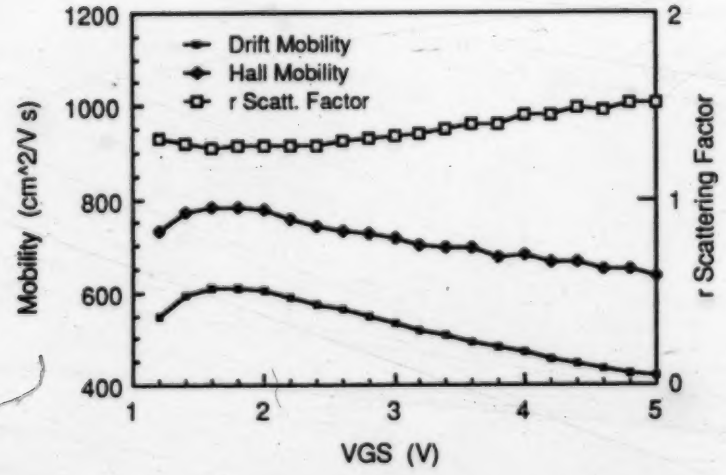

Fig. 4.71 Hall mobility, drift mobility, and scattering factor as a function of V_{GS}. The device is a wide MAGFET, (W/L=100μm/25μm), fabricated via Northern Telecom.

5. VERTICAL HALL DEVICE RESULTS

In Figs. 5.1 and 5.2 the relative current imbalance of the VHD is plotted against magnetic field. In Figs. 5.3 and 5.4 the Hall voltage is plotted, while in Figs. 5.5 and 5.6 it is the Hall voltage normalized to the voltage at the centre terminal. All these graphs are typical of the ten short, and ten long Northern Telecom VHDs tested.

5.1 Discussion

We first consider the percentage current imbalance for the short contact VHD, (see Fig. 5.1). Correcting for the current offset at zero field, the average relative imbalance at 1.0 T is about 1.1%. Over the range of 10 μA to 1 mA it changes less than ±6% from this average value. It is obvious that the 10 μA range should be avoided. At this level offsets are quite large and the data deviates considerably from the best fit line. Much the same can be said for the long contact VHD, (see Fig. 5.2). Its relative imbalance is approximately 4.0% at 1.0 T, straying less than ±3% from this figure over the current range indicated. Its lowest current level 0.1 mA, also suffers large current imbalances at zero field. Both VHDs exhibit a virtually linear response to the magnetic field, particularly at the higher current levels. The percentage deviation of the data from the best fit line is usually less than 2%.

For both VHDs the graphs of Hall voltage versus field strength indicate a practically linear response, (Figs. 5.3 to 5.4.). The data points usually deviate less than 1% from the best fit lines. Neglecting any offsets we can see

from these graphs that $V_H \propto IB$. This relationship is essentially equivalent to equation (2.2) for the long Hall plate. To account for the geometry of the VHD we would only have to introduce a geometric constant into equation (2.2). The VHD's sensitivity in terms of Hall voltage can also been defined as per equation (2.11). From the graphs in Figs. 5.3 and 5.4 this is merely the slope divided by the current level. This yields average sensitivities over the tested current ranges of, 25.3 V/AT and 64.3 V/AT for the long and short VHDs respectively. With this definition of sensitivity the short VHD is superior, while in terms of current imbalance the long VHD is superior. Graphs 5.5 to 5.6 are for the same data with the sensitivity expressed as per equation (2.12), the normalizing voltage being that at the central terminal. The virtually linear characteristics can be noted again. From these graphs the respective average slope for the long and short VHDs are 6.9 (1/T) and 3.4 (1/T). This would indicate that the long VHD is superior to the short, the opposite of what the sensitivity definition (2.11) gives. This disagreement will be dealt with in the following section.

5.2 Device Comparison and Sensitivity

One of the problems when working with magnetic field sensors is establishing a suitable definition of sensitivity. The percentage imbalance expression used for the dual drain MAGFETs seems attractive. The magnitude of the relative imbalance can range from 0.0 to 100%. The concept itself is quite intuitive and easily grasped, permitting an immediate comparison of the different geometries. For the VHD the sensitivity is expressed in three manners, as a percentage current imbalance, as the Hall voltage generated per Ampere-Tesla, or as the Hall voltage generated per Tesla referenced to

the applied voltage. In the first case the long VHD appears superior, at least if you are using current imbalance as the signal. If Hall voltage is the intended output signal the decision as to which VHD to use is not clear, since the second and third definitions do not favour the same VHD. Thus, there can be a difficulty in comparing similar devices. What of the task of comparing the MAGFETs to the VHDs? Is the comparison of the relative imbalance of the currents sufficient of does this neglect the possibility of the VHD being superior in the Hall voltage mode?

We will first consider the implication of some sensitivity definitions as applied to a long unipolar rectangular Hall sample. Combining equations (2.2), (2,5), and (2.6) we have;

$$V_H = r_n IB/nqt . \tag{5.1}$$

Using this equation with the sensitivities defined via equations (2.10) and (2.11) we get;

$$S_A = \partial V_H/\partial B = r_n I/nqt . \tag{5.2}$$

$$S_{RI} = (1/I)(\partial V_H/\partial B) = r_n/nqt . \tag{5.3}$$

For a fixed current level and geometry the absolute sensitivity equation (5.2), stresses the importance of carrier concentration. As n decreases the sample resistance increases resulting in a higher applied voltage. Figure 2.2(a) for a long Hall plate can accommodate a variable n by simply scaling the voltage difference between equipotentials, provided that n has no effect on mobility. In the case of fixed current and geometry the sample of lower carrier

concentration would have the higher power consumption. The sensitivity via equation (5.3) is also dependent on the sample resistance or resistivity. Note that the units are Ω/T.

Using the relations, $R=L/\sigma Wt$, $\sigma=nq\mu$ and $I=V/R$, equation (5.1) can be expressed in terms of the applied voltage;

$$V_H = \mu^*(W/L)BV \,. \tag{5.4}$$

Here R represents the sample resistance, σ the conductivity and V the applied voltage. Applying the definition of sensitivity as per equation (2.12) we obtain from equation (5.4);

$$S_{RV} = (1/V)(\partial V_H/\partial B) = \mu^*(W/L) \,. \tag{5.5}$$

With this definition the carrier concentration does not appear, and the units are 1/T. For a fixed geometry the material Hall mobility now becomes the critical factor. Furthermore at a given applied voltage the power consumption will be greater for the sample with higher mobility.

As shown, a judicious definition of sensitivity, together with a favourable carrier concentration or mobility, can ameliorate the sensitivity of a Hall plate, the same holds true for the VHD since it is merely a deformed Hall plate. With any given technology the major purpose of design is to maximize performance. This is usually achieved by altering the geometry of a device since it is the only remaining variable for the designer. In this case the different geometries can be compared with any convenient definition of

sensitivity. However, defined sensitivities that do not circumvent the effect of low carrier concentration can make the comparison of devices made with different technologies misleading. A possible means of getting around this difficulty is by specifying the sensitivity at a given power. For instance, with V_H as the desired signal the sensitivity to magnetic field is, $S_A = \partial V_H / \partial B$, however, the device power requirement must be stipulated. Device sensitivities can then be compared, but only at the same power level. It would seem that this method could be aided by normalizing the sensitivity with respect to the power, $S = (1/P)\partial V_H / \partial B$. However, if we consider what this does in the case of the long Hall sample, we can see that we run into other problems:

$$S_A = \partial V_H / \partial B = I / nqt , \tag{5.8}$$

$$S_A / P = S_A / VI = 1 / nqtV. \tag{5.9}$$

A lower power requirement implies a lower applied voltage. Thus, figures of sensitivity normalized to power can be made very high simply by operating at low power levels. Hence the necessity to refer to the same power level when comparing devices.

We now have several definitions of sensitivity which will be put to use to compare four vertical Hall devices. They are the Popovic VHD [4], the long and the short VHDs tested in this work and a numerically modelled VHD [3]. The Popovic design is not a simple VHD. It is realized on a CMOS process in the n-substrate, with a rectangular p doped ring which sorrounds the five contacts. The purpose of the ring is to modulate the effective device

thickness. In the numerical modelling of the device the contacts are assumed to be infinitely long, reducing the problem to two dimensions. Other assumptions are an electron mobility of 1350 cm^2/Vs, a typical value for bulk silicon, and $\mu^*B = .2$.

From Table 5.1 we are at liberty to compare the devices on the basis of the mentioned sensitivities. In terms of relative current imbalance the long and modelled VHDs appear superior. When the relative voltage imbalance is considered the long and modelled VHDs are again superior, followed by the Popvic and the short VHD. At this point we could reason that the long VHD is the sensor to choose whether voltage or current imbalance is employed. Furthermore we could say that the numerical modelling fairly accurately predicts the performance of the long VHD. As soon as we consider sensitivity in terms of Volts per Ampere-Tesla almost everything is reversed. The Popovic and the modelled VHD are by far superior. Their figures are about six times higher than the short VHD and over fifteen times higher than the long VHD. Also, the numerical model is in better agreement with the Popovic device. Even in terms of Hall voltage per Tesla the ranking is the same. Note though that for the long and short VHDs operating at lower power levels their sensitivities become drastically lower.

If the Hall voltage per Tesla is normalized with respect to power, again the long and short VHDs are inferior. What is worth noting is that with this definition the figure increases for lower power levels, as was mentioned for the long Hall plate. In the last columns the sensitivity of Hall voltage per Tesla ($\partial V_H/\partial B$), and current imbalance per Tesla ($\partial I_H/\partial B = \partial(I_1 - I_2)/\partial B$), are determined for the devices operating at a power level of 0.3 mW. This was the power consumption of the Popovic device and all others were adjusted to this

level. In terms of Hall voltage the sensitivities of the Popovic and modelled VHDs are respectively 3 and 4 times higher than the other two VHDs. At this power level the long and short VHDs are comparable at about 25 mV/T. With this definition the result is that the long and short VHDs are not at any real advantage to one another. At a given magnetic field and power level the same Hall voltage can be produced, a somewhat puzzling result. For the long VHD with its lower input impedance this means high current and low voltage at the input. For the short VHD it is low current and high voltage at the input. Even though the long VHD has the lower terminal voltage it generates the extra Hall voltage by virtue of the fact that it has the higher relative voltage imbalance. When the comparison is made in terms of current imbalance the long VHD is four times more sensitive than the modelled VHD. Unfortunately Popovic did not use current imbalance as a means of detecting magnetic field so no comparison is possible. Although the long and short VHDs are comparable in terms of Hall voltage the former is almost seven times more sensitive than the latter in terms of current imbalance. A must, since it operates at higher current levels and has a higher relative current imbalance.

If anything Table 5.1 shows the problems associated with comparing device sensitivity, and this is only for one specific device. The definitions in the first three columns have the advantage of being almost independent of power level. The third though, escalates with decreasing carrier concentration. This makes identical devices fabricated on differently doped substrates appear different, particularly if no attention is payed to the power level. In these devices higher sensitivities in terms of current imbalance or Hall voltage per Tesla are easily accommodated by increasing the power level.

All things considered comparison of devices using these last sensitivities is equitable only at a common power level.

For sake of integrating such a device with any circuitry, aside from knowledge of the terminal characteristics, the relationship between power and sensitivity, and of course maximum power handling, should be known. For the long and short VHDs the sensitivities of Hall voltage and current imbalance per Tesla versus power level are shown if Fig. 5.7. In all cases the sensitivity is proportional to the square root of the power.

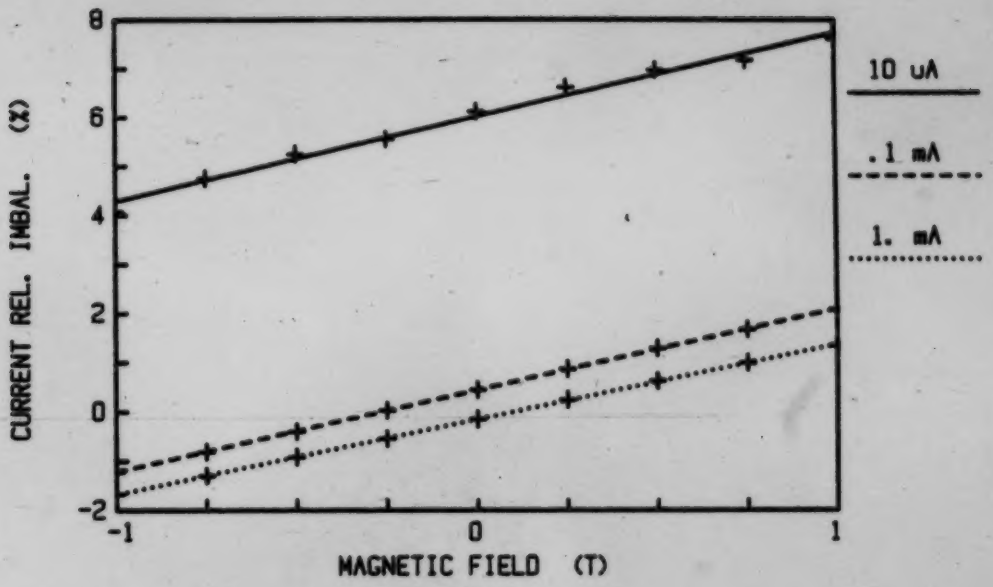

Fig. 5.1 Relative current imbalance as a function of magnetic field at various current levels, of the short VHD, fabricated via Northern Telecom.

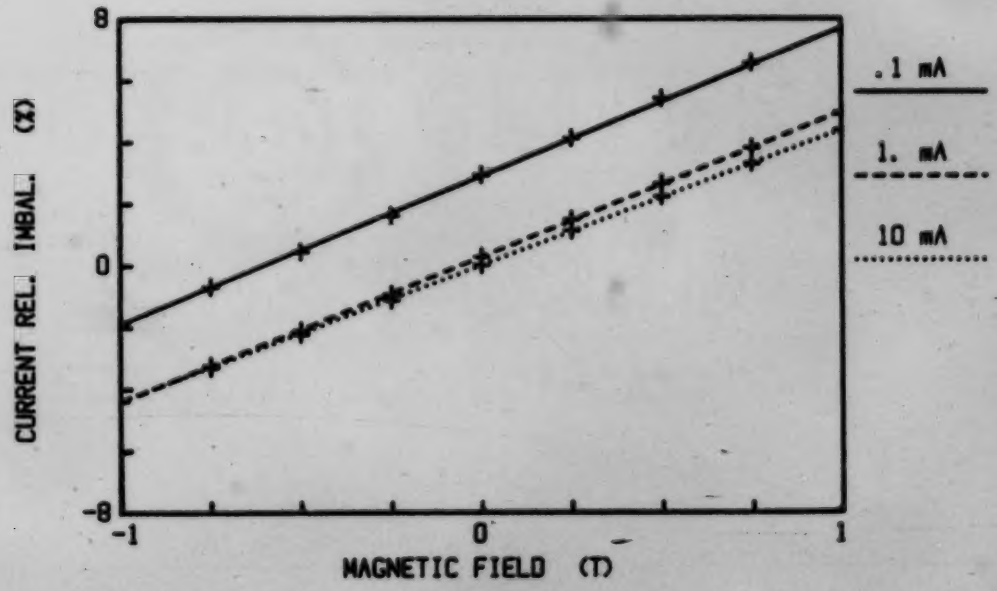

Fig. 5.2 As in Fig. 5.1, but for the long VHD.

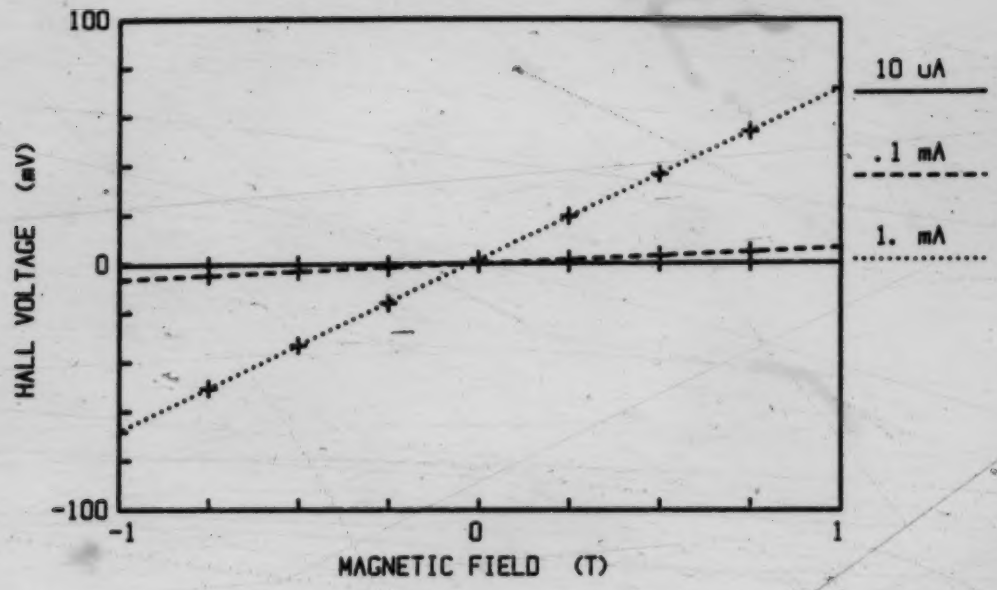

Fig. 5.3 Hall voltage as a function of magnetic field at various current levels, of the short VHD, fabricated via Northern Telecom.

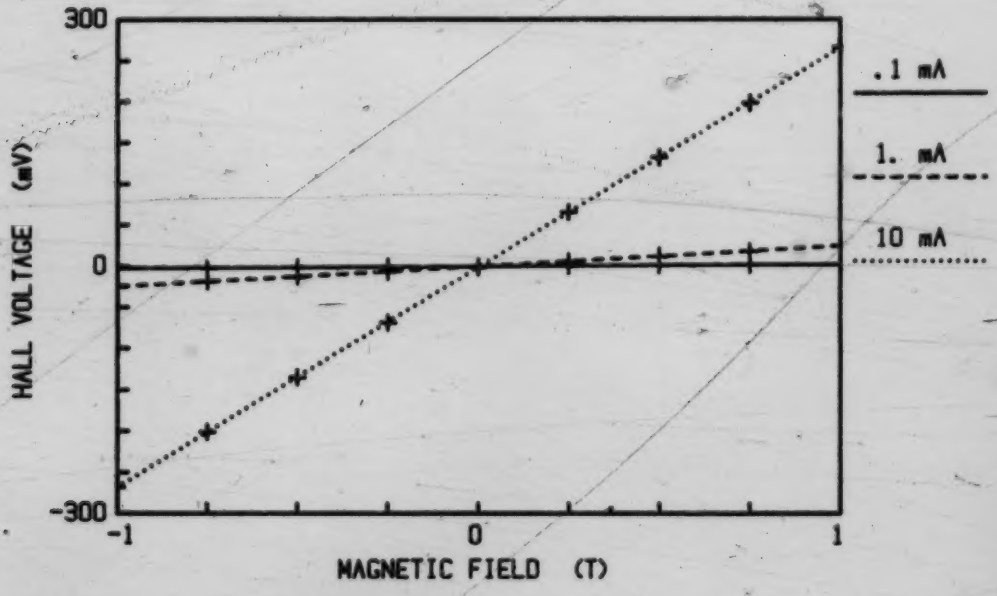

Fig. 5.4 As in Fig. 5.3, but for the long VHD.

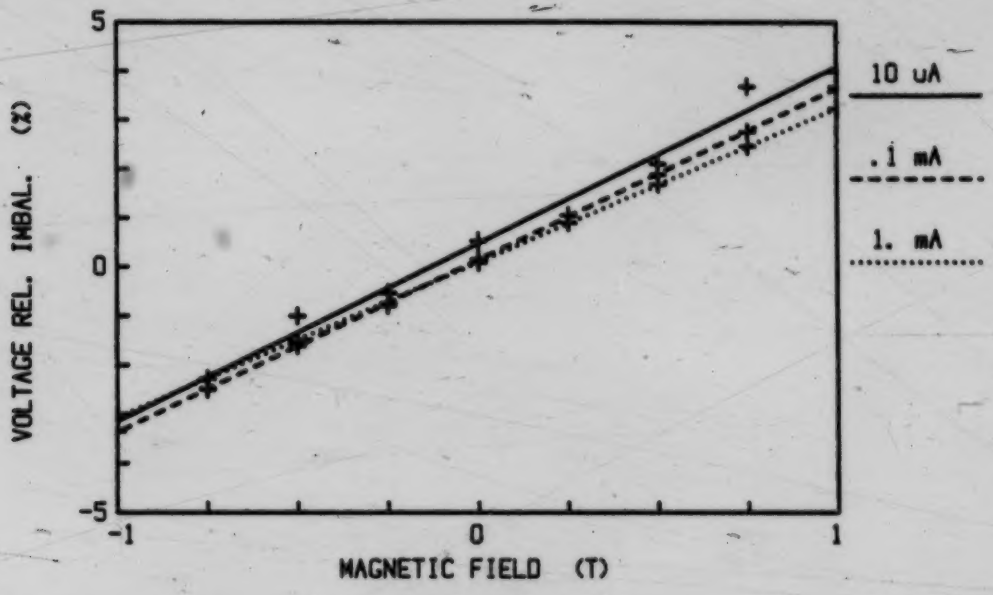

Fig. 5.5 Relative voltage imbalance as a function of magnetic field at various current levels, of the short VHD, fabricated via Northern Telecom.

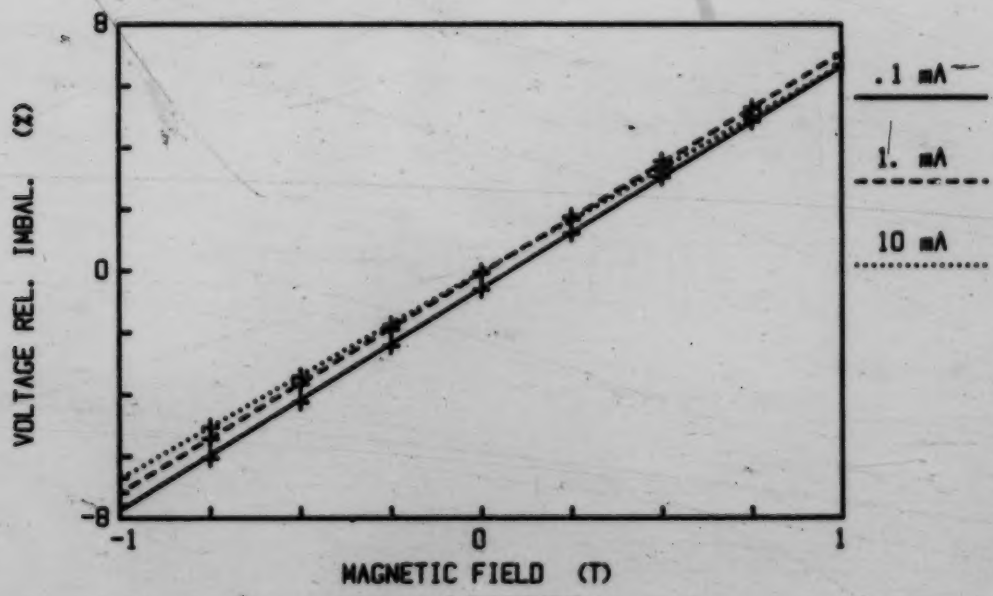

Fig. 5.6 As in Fig. 5.5, but for the long VHD.

Table 5.1 Comparison of device sensitivities

VHD	A	B	C	D	E	F	G	H
Numerical Model	4.77	6.70	420	67.0	.112	598	92.0	10.5
Popovic	___	4.70	350	70.0	.300	233	70.0	___
Long @ 1.0 mA	4.54	6.93	24.7	24.7	.352	70.2	22.7	41.7
Long @ 0.1 mA	4.52	7.18	24.5	2.45	.003	743	23.4	43.1
Short @ 1.0 mA	1.52	3.23	66.6	66.6	2.03	32.9	25.7	5.85
Short @ 0.1 mA	1.65	3.59	65.0	6.50	.018	355	26.7	6.75

A; $I^{-1}(\partial(I_1-I_2)/\partial B) \times 100$ [1/T]

B; $V^{-1}(\partial V_H/\partial B) \times 100$ [1/T]

C; $I^{-1}(\partial V_H/\partial B)$ [V/AT]

D; $(\partial V_H/\partial B)$ [mV/T]

E; Power [mW]

F; $P^{-1}(\partial V_H/\partial B)$ [1/AT]

G; $(\partial V_H/\partial B)$ [mV/T] @ 0.3 mW

H; $(\partial(I_1-I_2)/\partial B)$ [μA/T] @ 0.3 mW

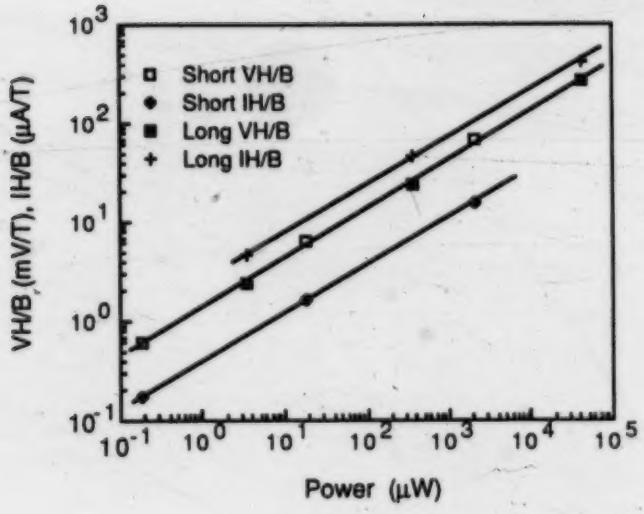

Fig. 5.7 Sensitivity, in terms of V_H/B and I_H/B, versus power, for the two VHDs.

6. A CIRCUIT MODEL OF THE DUAL DRAIN MAGFET

6.1 Model Construction

In the absence of a magnetic field with its two drains at equal voltage levels the MAGFET behaves like a regular MOS transistor. Hence it can be thought of as two MOSFETs in parallel. Each one has the same channel length as the MAGFET, but only half the width. An applied magnetic field produces an imbalance in the drain currents. Thus between the two drains we can place a magnetically dependent ideal current source, of value $I_H/2$ as shown in Fig. 6.1 [29]. This current source augments one drain current and diminishes the other by the same amount, causing a difference in the drain currents I_{D1}-I_{D2}=I_H. Actually the gate, source, and substrate contact of one transistor are connected to the corresponding contact of the other transistor. Since the impedance of an ideal current source is infinity the drains are isolated from one another. However the two transistors are connected or coupled by virtue of the fact that they abut along their channel length. This coupling can possibly be modelled by some effective resistance between the drains.

To determine the resistance as seen from between the drains the MAGFETs are connected as in Fig. 3.4. The voltage on drain one is fixed at 5.0 V while the voltage on drain two varied from 0.0 to 8.0 V, in 0.2 V increments. The gate voltage varies from 2.0 to 6.0 V in increments of 1.0 V. The source and substrate contacts are connected to ground.

The results of these measurements for the 100 μm x 100 μm MAGFET are

shown in Fig. 6.2, which is a plot of the difference in the drain currents (I_{D1}-I_{D2}) versus the difference in the drain voltages (V_{D1}-V_{D2}). These curves bear some semblance to the D.C. characteristics of a MOS transistor. If a family of MOS curves are mirrored and translated so that the saturation region portions of the response coincide on the horizontal axis the result would be identical to Fig. 6.2. With both drains at 5.0 V and (V_G-V_T)≤5.0 the drains are surrounded by a depletion region and the two transistors are in the saturation region. Ideally, in this situation the drain currents should be equal. When V_{D2} is grounded, (V_{D1}-V_{D2})=5.0 V, the current difference between the drains is very large. Drain two loses its depletion region and contacts the inversion layer directly. It then acts as another source contact. The MAGFET becomes a MOSFET of rather unusual geometry. As the voltage on drain two is raised above ground the differential current decreases. This is caused by two effects. Firstly with V_{D2}>0.0 there is positive current flow from drain two to the source. Secondly current flow through the transistor formed by drain one and drain two decreases. Since drain two acts as a source it is now at a higher potential than the substrate. This increases the threshold voltage of the transistor lowering the current flow as the gate voltage is fixed. As V_{D2} increases these effects intensify, further reducing the differential current. Eventually the transistor formed by the two drains is turned off. A depletion region forms around drain two saturating the current flow from drain two to the source. For further increases in V_{D2} the depletion region around drain two merely grows. The path between the two drains is effectively one of high resistance. For V_{D2}>V_{D1}, corresponding to

$(V_{D1}-V_{D2})<0$, differential current flow is practically zero.

The incremental resistance between drains is the inverse of the slope of the curves in Fig. 6.2. The resistance is plotted in Fig. 6.3. The threshold voltage for these devices is slightly less than 1.0 V. Since $V_{D1}=5.0>(V_G-V_T)$, the transistor formed with this drain is always in the saturation region. When $V_{D2}>(V_G-V_T)$ then presumably the other transistor is also in the saturation region. At the point when $V_{D2}=(V_G-V_T)$ the incremental resistance between drains becomes quite large increasing even more as V_{D2} increases. The corresponding graphs of $(I_{D1}-I_{D2})$, and incremental resistance between drains versus $(V_{D1}-V_{D2})$ for the other dual drain MAGFET geometries can be found in Appendix C. Appendix C also contains plots of the output resistance versus bias point of the dual drain MAGFETs operated as MOS transistors.

From these results it is possible to construct a low frequency small signal equivalent circuit model of the dual drain MAGFET [29]. A possible circuit is shown in Fig. 6.4. Its various components will be discussed for the D.C. bias condition that the two drains are at the same voltage, high enough to place the MAGFET in the MOS saturation region of operation. The resistances r_{o1}, and r_{o2} represent the output resistances of the two transistors. Ideally they should be equal. Their value should essentially be twice the output resistance of the MAGFET operated as a MOSFET. The usual transistor transconductance g_m does not appear since no small signal gate signal is applied. The resistance r_{DD} in parallel with $(r_{o1}+r_{o2})$ is the incremental

resistance at the point $(V_{D1}-V_{D2})=0.0$ in Fig. 6.3. To calculate r_{DD} one must know r_{o1}, r_{o2}, and the value of this incremental resistance. The quantity g_b is, for lack of a better word, the magnetic transconductance;

$$g_b = \partial I_H/\partial B. \tag{6.1}$$

The units of g_m are $1/\Omega$, which is conductance, while for g_b they are A/T. To obtain $I_H(B)= I_{D1}(B)-I_{D2}(B)$ the MAGFET is operated at equal and fixed drain voltages with the magnetic field B varying. This is precisely how the relative imbalance is measured as a function of B. The magnetic transconductance can then be written as;

$$g_b = (I/I)(\partial I_H/\partial B) = I(\partial(I_H/ I)/\partial B) = I(\partial\delta/\partial B). \tag{6.2}$$

The sum of the two drain currents is represented by I. As seen from previous measurement results, at a given operating point $(\partial\delta/\partial B)$ is for most purposes a constant.

The steps involved in equation (6.2) are valid provided the total current I is independent of magnetic field. The dependence of total current on magnetic field has been investigated. One Northern Telecom dual drain MAGFET of each geometry was tested. The general result is that at a field strength of +1 T or -1 T the total device current decreases from the current level at zero magnetic field I(B=0). The relative change in current, $(I(B=\pm 1)-I(B=0))/I(B=0)$, over the same range of biasing voltages used in other

tests, is usually less than -1%. The absolute difference of the relative change in current at +1 T and -1 T is typically about .1%. This small difference is the resolution limit of the semiconductor parameter analyser. The fact that total current changes with magnetic field, whether the MAGFETs are in the MOS linear or saturation region, is a magneto-resistance effect. As mentioned in section 2.1 this is possible even if the mobility in the inversion layer is isotropic and only one carrier type is present [5]. For purposes of developing a small signal model this magneto-resistance effect can be neglected. In the next section it will be seen that there are other effects, that more strongly affect the accuracy of the model.

6.2 Model Application

The MAGFET is a very versatile electronic magnetic field sensor. The support and signal processing circuitry it requires will be a function of the manner in which it is used, and the final form of the output signal required. For instance there is the MCO, a magnetically sensitive voltage controlled oscillator [30]. In this device the field dependent current of one drain charges or discharges a capacitor. The corresponding change in the capacitor voltage is ultimately converted into a frequency. Another design replaces the two usual pair of MOS transistors in a CMOS differential amplifier with two complementary dual drain MAGFETs [1]. The drains are cross coupled. The drain of one MAGFET with increasing current is connected to the drain of decreasing current in the other MAGFET. With this arrangement small imbalances in the drain currents produce large output voltage variations

Since the current imbalance from a MAGFET is small some degree of

amplification is desirable. This can be achieved by employing conventional or merged amplifiers [1]. A MAGFET is a merged amplifier since it can simultaneously detect magnetic field and amplify the signal. This is possible when the MAGFET is working in saturation, and is the essence of the design by Popovic and Baltes. To achieve simultaneous sensing and amplification it is possible to get by with a single MAGFET. It is also possible to replace the pair of MOS transistors in a differential amplifier by a single MAGFET, because of its dual drain structure.

Consider the characteristics of an ideal dual drain MAGFET at zero field with the two drain voltages being equal. The two drain currents are equal hence we see only one line, (see Fig. 6.5 (a)). In the saturation region the expression for the drain to source current is [30];

$$I_D = (KW/2L)(V_G - V_T)^2(1-\lambda V_{DS}) , \tag{6.3}$$

$$\lambda = 1/V_A . \tag{6.4}$$

The term λ is known as the channel length modulation parameter. The quantity V_A is analogous to the Early voltage in bipolar transistors. It represents the point of intersection of the V_{DS} axis and the line tangent to the saturation region of the response. The final term on the right hand side is a correction to account for the small increase in drain current with V_{DS}. The current in any one of the two drains is half of equation (6.3). With the application of a magnetic field one drain current increases while the other

decreases. We will then see two lines, their separation increasing with increasing field. If equal resistive loads are introduced between the each drain and its voltage supply we can draw a single load line as shown in Fig. 6.5 (b). The intersection of the load line and a current line gives the operating value of drain current and voltage. As can be seen this results in a voltage difference at the drains. It can now be appreciated that even small current imbalances, used in conjunction with the MOS structure operating in the saturation region, can produce sizeable voltage differences. The amount of voltage imbalance at a fixed field will depend on the current imbalance, the slope of the current lines in the saturation region and the slope of the load line. If the MOS channel were merely a uniform conducting slab of silicon separate circuitry would be required to produce the same voltage levels.

The previous discussion was a simplified illustration of how a single MAGFET can be used to produce large signal levels. Determining the drain voltage difference graphically from Fig. 6.5 (b) would be in error. The original current lines were obtained on the basis of the two drain voltages being equal. The voltage difference caused by the intersections with the load line violates this condition. The picture presented is instructive, but not good enough for quantitative discussion. For determining the response $(v_{D1}-v_{D2})$ to varying magnetic field we can use the small signal model developed in the previous section. If the two drains have the same value of load resistance the expression for the differential voltage per tesla becomes;

$$(v_{D1}-v_{D2})/\Delta B = -g_b /(1/r_{o1} + 1/R_L + 2/r_{DD}). \qquad (6.5)$$

Using equation (6.2) this becomes;

$$(v_{D1}-v_{D2})/\Delta B = -I(\partial\delta/\partial B)/(1/r_{o1} + 1/R_L + 2/r_{DD}). \qquad (6.6)$$

In deriving (6.5) from the small signal model it was assumed that $r_{o1}=r_{o2}$. The quantity ΔB represents a small change in magnetic field. We can also make use of a result from the MOSFET small signal model [31];

$$r_o = V_A/I. \qquad (6.7)$$

Where r_o is the output resistance of the MOSFET in saturation. In the previous section it was mentioned that $2r_o=r_{o1}$. Equation (6.6) can then be rewritten as;

$$(v_{D1}-v_{D2}) = -(2V_A/r_{o1})(\partial\delta/\partial B)/(1/r_{o1} + 1/R_L + 2/r_{DD}). \qquad (6.8)$$

If the drains of the MAGFET are connected to current sources of very high impedance then the the term $1/R_L$ in equation (6.8) is negligible. Furthermore, if $r_{DD}>>r_o$ the expression reduces to ;

$$(v_{D1}-v_{D2})/\Delta B = -2V_A(\partial\delta/\partial B). \qquad (6.9)$$

The result can be justified intuitively by recalling the earlier graphic

explanation. Large voltage differences will be produced for a large V_A, (i.e. flatter lines in saturation.), and a greater relative imbalance. The requirement that $r_{DD} >> r_o$ isolates the two transistors in the model. This last expression is inappropriate for the same reasons as given for calculating the voltage difference graphically.

To measure the drain voltage imbalance as a function of magnetic field the MAGFET is connected as in Fig. 6.6. The drains are driven by current sources, 80.0 μA for drain one and 80.5 μA for drain two. This small current imbalance helps reduce the zero field drain voltage imbalance. The corresponding gate voltage at this current level is about 5.0 V. Figure 6.7 shows the measured drain voltage imbalance, for $|B| \leq 100$ G (10^4 G=1 T), for a Northern Telecom 100 μm x 100 μm dual drain MAGFET.

Since the impedance of the analyser's current source is much greater than r_{o1} and r_{DD} the load impedance is neglected in equation (6.5). The calculated response comes close to the measured response. Although, it appears that the measured data is better approximated by two differently sloped lines in the different field directions. It must be remembered that in the model the resistance values are assumed constant. From the resistance plots in Fig. 6.3 it can be seen that this is not true. As $(V_{D1}-V_{D2})$ increases the incremental resistance between drains decreases, and vice versa. From equation (6.6) it can be seen that higher resistances produce higher voltage differences, and that lower resistances produce lower voltage differences. This helps explain the discrepancy between the measured and the calculated response. To obtain better agreement for drain voltage differences as small

as 0.2 V the incremental resistance between drains could be assumed to vary linearly with the drain voltage difference.

The drain voltage imbalance for larger field strengths is shown in Fig. 6.8. The characteristics are now bowed. At -.1 T = -10^3 G, where the voltage difference is about 1.5 V, the second drain is more than one threshold level below the first drain. At this point the MOS transistor formed by the two drains has not been activated. Its source voltage, which is V_{D2}, is well above the substrate, giving it a $V_T > 0.9$ V. If we refer back to Fig. 6.2 we can see that for $V_G = 5.0$ V large current differences start for a voltage difference in the neighborhood of 2.0 V. At this point the conditions under which the model is derived are violated making it invalid. At positive fields when $V_{D2} > V_{D1}$, the incremental resistance between drains increases, increasing the magnitude of the drain voltage difference as indicated by equation (6.6). This of course can not continue indefinitely as eventually the voltage on drain two will be high enough to cause breakdown, and again the model becomes invalid.

The design of Popovic and Baltes produced sensitivities of 1.2 V/T at 10.0 V and 100 μA supply. Comparatively a single dual drain MAGFET has yielded better than 15.0 V/T at 5.0 V and 160 μA supply. The power consumption is about the same, however the power requirement of the current sources has not been considered here. To make room for them the operating voltages of the MAGFET can be reduced. From equation (6.6), this will actually improve the figure of 15.0 V/T. At lower gate voltages the resistances r_{DD} and r_o will increase.

The limitations of a sensor circuit realized in such a manner is

linearity, and range of response. For small fields the response is quite linear, but not the same in different field directions. Beyond field levels of 0.01 T the response deviates considerably from a straight line. For the bias conditions used here, the field level beyond which the second drain loses it's depletion region is about -0.1 T. At lower gate voltages this would occur at even smaller values of negative field, further restricting the useful range of the device. Some of these deficiencies could be overcome by connecting the gate to a separate voltage source and operating the MAGFET deeper in the saturation region. This would make the response more symmetric. However, since the output resistances change appreciably with the drain voltage difference, the response would undoubtably be nonlinear. These problems can be avoided by making the load resistance far smaller than the model resistive elements, but at the cost of lower amplification.

The ever present problem at low fields is of course noise. At zero field the device tested has an averaged voltage imbalance of 132 mV. During an observation period of about one minute the fluctuations are between 95 mV and 170 mV. This 75 mV range corresponds to about 0.05 T from the graph in Fig. 6.7. As the test environment was not designed to provide noise shielding this figure gives a quick estimate of a detectable lower magnetic field limit, if the signal is not averaged to reduce noise.

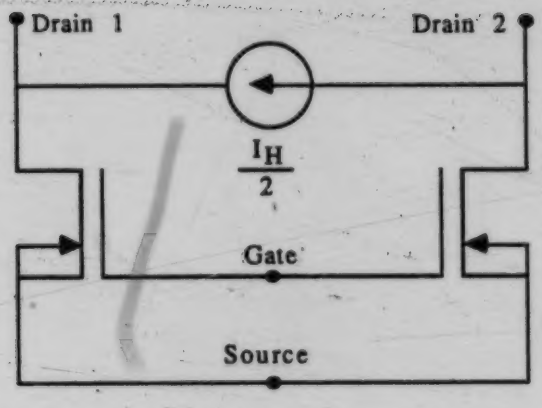

Fig. 6.1 Circuit model of the dual drain MAGFET, with equal voltages on the drains.

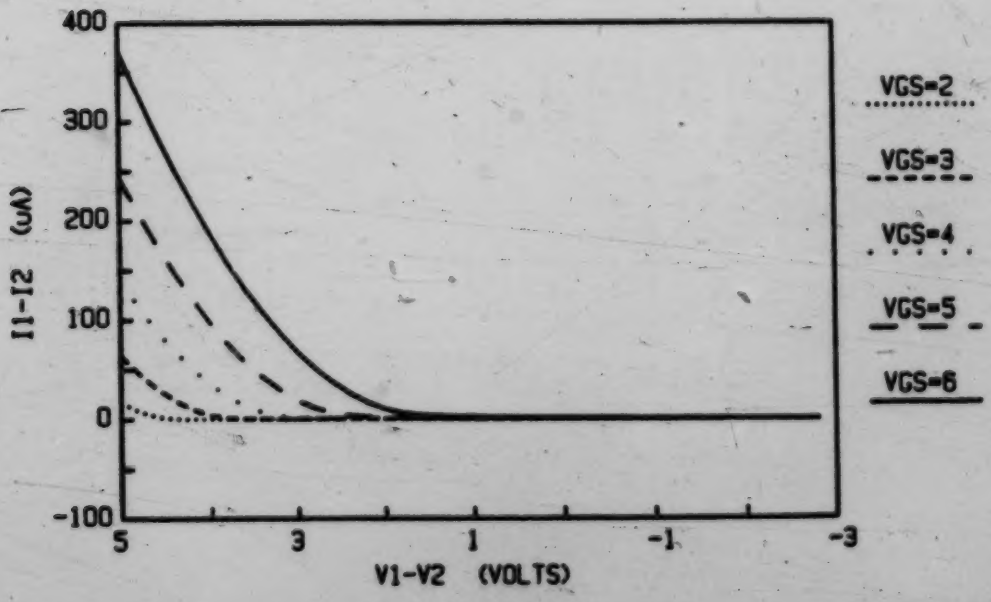

Fig. 6.2 Drain current difference versus drain voltage difference for the square dual drain MAGFET (W/L=100μm/100μm), fabricated via Northern Telecom. (I1-I2)=(I_{D1}-I_{D2}), (V1-V2)=(V_{D1}-V_{D2})

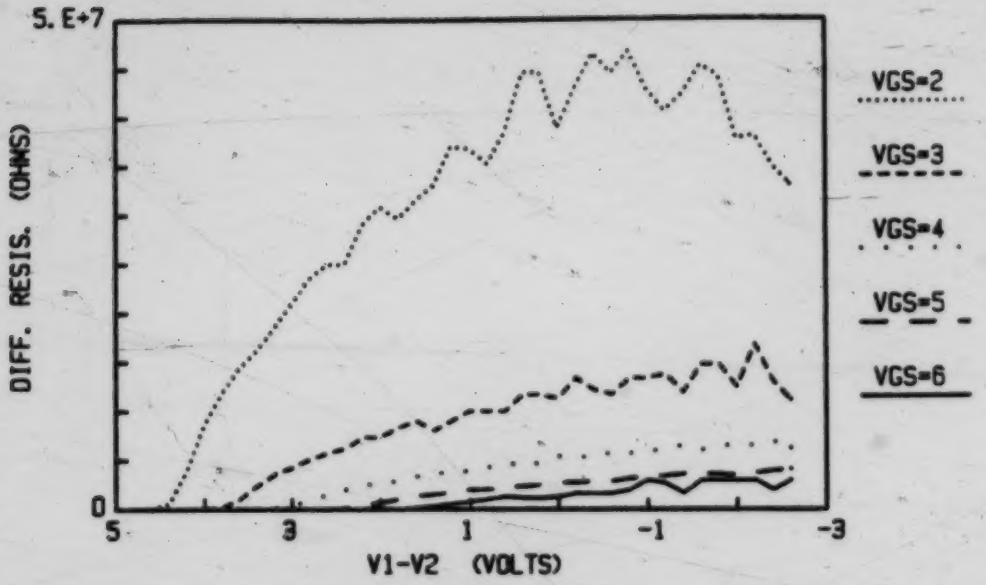

Fig. 6.3 Incremental resistance between drains for various operating points of the square dual drain MAGFET (W/L=100μm/100μm), fabricated via Northern Telecom.

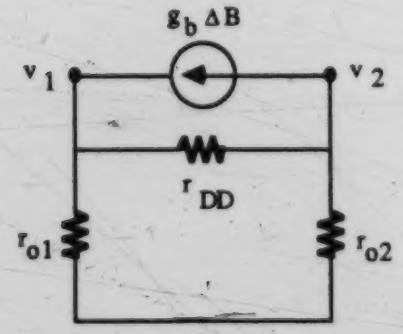

Fig. 6.4 Small signal model of the dual drain MAGFET in the MOS saturation region.

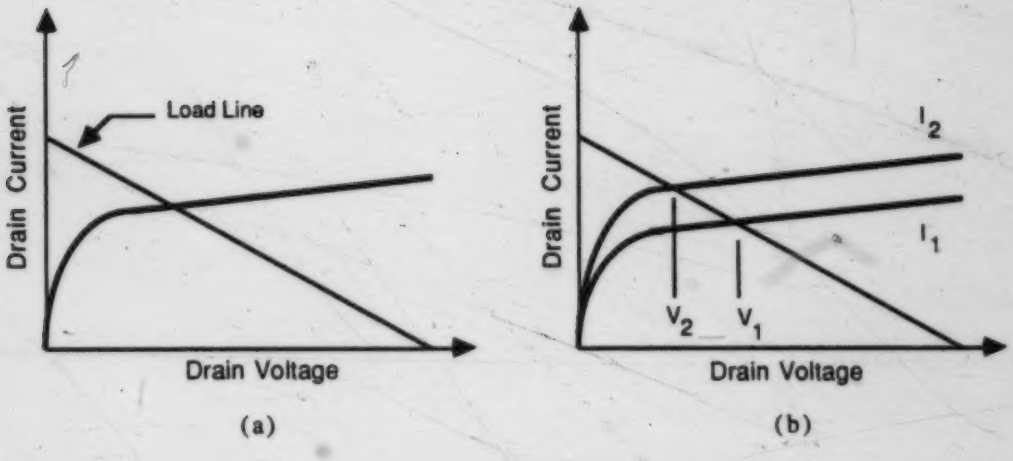

Fig. 6.5 Intersection of the MAGFET I-V characteristics with a load line, (a) drains with equal currents (B=0), (b) drains with unequal currents (B≠0).

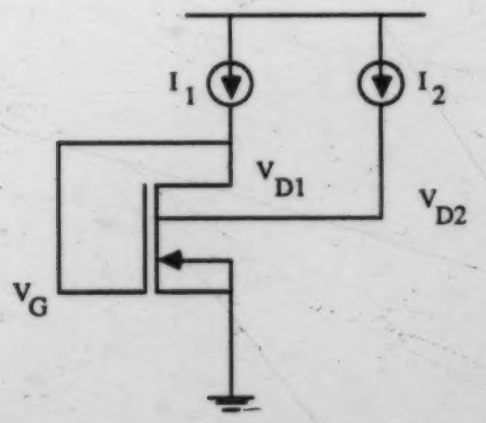

Fig. 6.6 Biasing circuit for using the drain voltage difference of the MAGFET as a measure of the magnetic field.

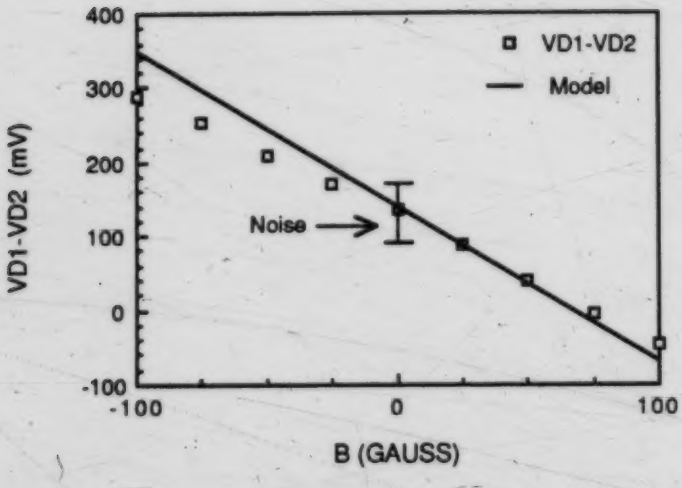

Fig. 6.7 Drain voltage difference versus magnetic field. The device is the Northern Telecom square MAGFET (W/L=100μm/100μm), in the MOS saturation region.

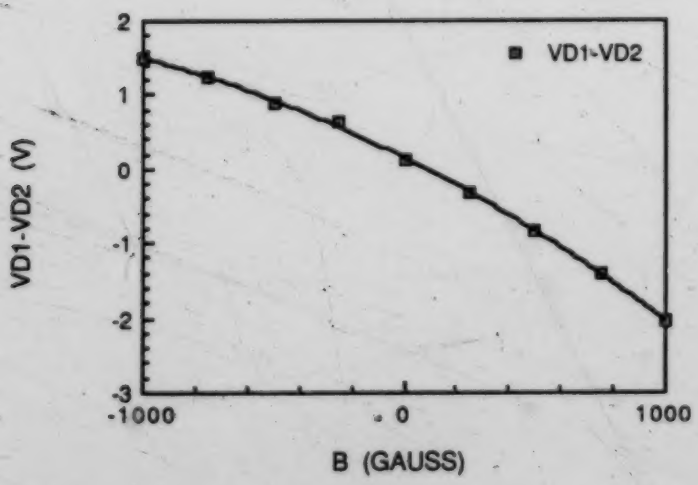

Fig. 6.8 As in Fig. 6.7, but for stronger magnetic field.

7. MAGFET NOISE RESULTS

7.1 General Noise Behaviour

With the first group of noise spectra, Fig. 7.2, we can compare the total measured noise voltage power spectral density (PSD), (device plus measurement system), to the noise PSD of the measurement system alone. The two lower spectra are for the noise from the measurement system using the differential and single input amplifiers. The measurement system being comprised of an amplifier and the spectrum analyser, (see section 3.5). These spectra are referenced to the amplifier input to permit immediate comparison to the noise measured with the device connected to the amplifier. It is possible to represent a linear two-port as a noiseless two-port with two external noise generators completely describing the noise output of the original noisy two-port [32, 33, 34], (see Fig. 7.1). To obtain the equivalent input noise voltage and noise current generators, noise measurements were performed with the amplifier inputs open circuited and short circuited. Since only a rough estimate of the measurement system noise level is required it is assumed that the two noise generators are uncorrelated [35].

The two upper spectra in Fig. 7.2 are the noise voltage PSD from a single drain and from between drains. They are from the large square MAGFET operating in the MOS linear region. For this device and bias conditions the measurement system noise is only appreciable, as compared to the total measured noise, near .1 Hz and at higher frequencies where the spectra flatten out, f $>10^3$ Hz. Between these frequency extremes the measurement system noise is considerably less than the total measured noise. The total

measured noise can then be considered to be equivalent to the total device noise. In the spectra to be presented here the devices are all biased in the MOS saturation region, with the result that the noise levels are far greater than the measurement system noise shown in Fig. 7.2. Thus, in most calculations the system noise can be disregarded.

From Fig. 7.2 we observe that below 100 Hz the device noise spectra have an approximate 1/f dependence. Another point to note is that the PSD for the noise from the drain voltage difference is consistently higher then the PSD for the noise from the single drain up to about 10 kHz. Beyond 10 kHz if we account for the noise of the measurement system the device noise spectra will drop about 0.5 dB for the differential drain noise, and about 2.2 dB for the single drain noise. Consequently the difference noted above is preserved up to 100 kHz. This argument can also explain the discrepancy at 0.1 Hz.

The spectra in Figures 7.3 to 7.5 are for the square, long, and wide channel Northern Telecom dual drain MAGFETs respectively. In each graph there are five noise voltage PSDs. They are;

(V1-V2)^2 = The average noise voltage PSD from the drain voltage difference, using the differential amplifier.

(V1)^2 = The average noise voltage PSD from a single drain, with both drains loaded.

(V1+V2)^2 = The average noise voltage PSD from amplifying each drain noise voltage and then summing them.

(VSh)^2 = The average noise voltage PSD with the drains tied together.

(VFL)^2 = The average noise voltage PSD from one drain, with

that drain loaded and the other floating.

The underlying quantities V1, V2, VSh, VFL, are time stochastic voltages V1(t), V2(t), VSh(t), VFL(t). All of these spectra are referenced to the device output. That is to say that any measured PSD is adjusted by the amplifier gain.

For the square MAGFET, at each frequency point the following general trend is observed;

$$(V1-V2)^2 > (V1)^2 > (V1+V2)^2 > (VSh)^2.$$

This implies that the least noise is generated when the drains are tied together, so as to make the MAGFET operate as a MOSFET. If they are not tied together the generated noise is greater, regardless of how the drain output voltages are combined.

For the wide MAGFET the generalization at each frequency point is almost the same, except that $(V1+V2)^2 \approx (V1)^2$. As before the noise is the least with the drains tied. Once they are disconnected from one another the result is more noise.

As for the long channel MAGFET this observation seems valid within the smaller range of 1 Hz to 10 kHz. Outside this range the data of some spectra depart from an almost straight line behaviour. The most obvious spectra are $(V1+V2)^2$ and $(V1-V2)^2$. In the case of the latter after 10 kHz the spectrum drops very rapidly, with a slope of about -20 dB per decade. Below 10 kHz the slope is about -10 dB per decade. This 10 dB difference in slope is most likely caused by capacitive loading of the coaxial cables and the differential amplifier. The drain load resistors of the long channel MAGFET are 147.5 kΩ,

while for the square and wide MAGFETs they are 33.2 kΩ and 13.1 kΩ respectively. At 10 kHz 100 pF of capacitance has a reactance of about 150 kΩ. Comparatively the loading effect in these plots should be more evident for the long channel device. Indeed, it can be seen that for the square MAGFET the (V1-V2)^2 spectrum starts to decrease more rapidly at about 50 kHz, while for the wide MAGFET it is nearer 100 kHz.

The (V1+V2)^2 spectra are obtained by first amplifying each drain noise voltage and then adding them. The differential and single input amplifiers are used at the same time, and unfortunately their characteristics are not identical. Their low frequency 3 dB points are different. Below a few hertz the drain voltages are not amplified by the same amount, hence one drain voltage predominates and the (V1+V2)^2 spectrum rises to that of (V1)^2. The amplifiers have different input impedances, hence at higher frequencies one drain noise voltage decreases sooner as the drain becomes more loaded and again the (V1+V2)^2 spectrum rises to that of (V1)^2. This effect is also visible in the corresponding spectra of the square MAGFET.

In referencing the (V1+V2)^2 spectrum to the amplifier input there is the additional problem of which amplifier gain to use. The manufacturer specifies the gain as 60 ± .3 dB. From a few hertz to well over 100 kHz the measured gain is 59.8 ± .2 dB. If there is great disparity in the amplifier gains the resulting spectra can be seriously distorted, as explained earlier. Since the gains are quite close, within a few tenths of a dB, the distortion should not be too great. The measured spectra using a single amplifier are adjusted using the measured frequency dependent gain. To be consistent with this the (V1+V2)^2 spectra are adjusted using a constant gain of 59.8 dB. Using this constant gain and neglecting capacitive loading the (V1+V2)^2 spectra should

only be considered in the approximate intervals 10 Hz to 1 kHz for the long MAGFET, and 10 Hz to 10 kHz for the square and wide MAGFETs.

If in these log log plots the (VSh)^2 spectra below 1 kHz are approximated with straight lines the slope values lie between -.9 and -1.0, accounting for the factor of ten in the definition of a decibel. Around 10 kHz the spectra tend to flatten out and then fall rapidly again. This is a combination of the onset of the thermal noise level and capacitive loading. By adding the thermal noise PSDs of the MAGFET, circuit resistive elements, and measurement system the corner frequency can be estimated. The corner frequency is the frequency at which the extrapolated 1/f spectrum crosses the thermal noise level. At the corner frequency the actual spectrum should be about 3 dB higher than the thermal level. To calculate the thermal noise level of the MAGFETs the following expression is used [36];

$$\Delta i_n^2/\Delta f = 4kT(2W/3L)(\mu C_{ox}(V_{GS}-V_T)). \qquad (7.1)$$

Here k is Boltzmann's constant in Joules per degree Kelvin, T the temperature in degrees Kelvin, Δf the frequency bandwidth, and Δi_n^2 the resulting noise current power. The left hand side of equation (7.1) can be recognized as the noise current PSD. It can be converted to a noise voltage PSD if the device load impedance is known. This expression is appropriate for a MOSFET in saturation. It is applied to the MAGFET with drains shorted under the assumption that the drain separation does not affect the geometric factor W/L. The various thermal noise levels and corner frequencies are given in Table 7.1. At the corner frequencies, obtained using the total thermal noise

level, the (VSh)^2 spectra are about 3 to 4 dB greater than the estimated thermal levels. This substantiates, to a degree, the stated cause of the spectra flattening, and the calculation of the thermal noise level. As a point of interest the corner frequency using solely the device thermal noise level is included.

The spectra with drains shorted reveal a slight incongruency with the idea that under this condition the MAGFET can be considered a regular MOSFET. The equivalent input noise voltage and output noise current PSD of a MOSFET are inversely proportional to the channel area [36, 37, 38, 39, 40, 41]. From 1 Hz to 1kHz the average difference between the (VSh)^2 spectra of the square and the wide MAGFETs is 5.2 dB, the square having a lower noise level. Similarly, for the square and long MAGFET the average difference is 3.2 dB. Since the long and wide channel devices have 1/4 the area of the square channel their equivalent input noise voltage PSD should be 4 times higher. Using these average differences the input noise voltage PSD of the wide channel MAGFET is about 1.5 times that of the square, and for the long channel about 3 times that of the square.

7.2 Noise and Magnetic Field

The square MAGFET is the only device whose PSDs are measured while the device is in a magnetic field. The spectra measured are (V1-V2)^2 and (V1)^2. The field used is from a permanent magnet with a field strength of .27 T. The resulting spectra are indistinguishable from the zero field case.

The definition used in calculating the signal to noise ratio (SNR) is, (Root mean square noise voltage)/(Signal voltage). The minimum detectable field (B_{min}) is that which will produce a signal to noise ratio of one. Two

signals are used. The net voltage difference between drains, and the voltage change of one drain, with the application of a magnetic field. The root mean square (RMS) noise voltage is obtained from the appropriate noise spectrum at an arbitrary frequency of 1 kHz for a bandwidth of 1 Hz. To calculate B_{min} it is assumed the response to magnetic field is linear.

These various quantities are shown in Table 7.2. In terms of signal level or RMS noise voltage the long MAGFET is the highest followed by the square and then the wide MAGFET. The calculated SNR and B_{min} indicate that the square MAGFET is the better device of the three. The B_{min} of the long or wide MAGFET is about 2.5 times greater than that of the square. However, the area of the square MAGFET is 4 times the area of the wide or long MAGFETs. If these latter two devices are scaled up to the same area of the former a reduction in noise level can be expected, since the noise levels from MOSFETs are inversely proportional to channel area. The anticipated factor of 2 improvement in the B_{min} of the long and wide MAGFETs would make them almost equivalent to the square. Unfortunately we can not be too certain of this as it was mentioned in the previous section that the MAGFETs do not appear to steadfastly follow the inverse area rule.

An interesting result is that for these devices the SNR is relatively unaffected by whether the signal is the net voltage difference between drains or the change in voltage from a single drain. For each MAGFET geometry, over a suitable frequency range, the (V1-V2)^2 spectrum is about 6 dB greater than the (V1)^2 spectrum. This figure is obtained by averaging the difference at each frequency point. Six decibels translates to a factor of 4, meaning that the RMS noise voltage from a single drain is half the RMS

noise voltage from between drains. The signal from one drain is essentially half of that obtained from between drains, giving the same SNR. Since the (V1+V2)^2 spectra are generally lower than these other two it may seem advantageous to sum the drain voltage signals. Unfortunately the net change in voltage would be zero giving a SNR of value zero.

In practice measurement systems with a 1 Hz bandwidth are rare. For a more realistic value of B_{min} a larger bandwidth would be in order. By approximating the spectral frequency dependence with a straight line on the log log plot, the resulting function on a linear scale can be integrated over the required bandwidth to obtain the total noise power. Doing this for the square MAGFET we have B_{min}=70 μT for a bandwidth of .1 Hz to 10 kHz.

7.3 Spectra and their Relative Difference

One of the more bewildering results of the noise measurements is the relative difference between the (V1-V2)^2, (V1+V2)^2, and (V1)^2 spectra. For instance the difference between the (V1-V2)^2 spectrum and the (V1)^2 spectrum is about 6 dB, for each MAGFET geometry operating in the saturation region. Again this figure is the average of the difference at each frequency point over a valid frequency range. The difference at each frequency point varies. However, for each device the standard deviation for the 30 or more points averaged is less than .6 dB.

To check if this 6 dB difference was an artifact of the measurement technique, the following test was conducted for each MAGFET geometry. The two drains were tied together, forming a MOS transistor. Two such MOSFETs were biased to operate very near the bias point used in the other noise tests. The source and substrate contact of each transistor were connected to the

same ground point. The noise voltage PSD of each transistor drain was measured and also the noise voltage PSD from between the two drains. . The typical findings from each geometry are as follows. The spectra from the individual drains differ only slightly. From 1 Hz to 100 Hz the difference is usually less than 1 dB. From 100 Hz and up, barring any loading effects, the difference is usually less than .5 dB. In this latter frequency range the spectra are much smoother since a larger number of measurements were averaged. As for the spectrum for the difference in the drain voltages, it is on average 3 dB greater than either spectrum from an individual drain. If two uncorrelated noise sources with the same PSD are summed or subtracted the resulting noise PSD is twice the PSD of any one noise source. A factor of 2 is equivalent to 10xLog(2) on a decibel scale, which is approximately 3 dB. The 3 dB difference in this test was an anticipated result, since the two transistors are distinct their noise voltages should be uncorrelated. These findings imply that the noise measurement system is in order, and that the 6 dB difference is not a measurement artifact.

For the square MAGFET in the linear region the difference between the (V1-V2)^2 and (V1)^2 spectra behaves differently. In the flat portion of the spectra the difference is altered by the measurement system noise. Accounting for the measurement system noise brings the difference to under 3 dB. For the 1/f portion of the spectra the difference tends to increase as the frequency drops, but it does not reach 6 dB. Approaching .1 Hz the difference becomes difficult to establish as the spectra are more erratic because of the fewer number of averaged readings. Although these facts are tenuous they may indicate that the 6 dB difference is peculiar to 1/f noise mechanisms.

The spectra (V1-V2)^2 and (V1+V2)^2 contain information regarding

the cross spectral density of V1(t) and V2(t). To recapitulate, the spectra are produced by Fourier transforming a sampled time signal, squaring the spectral amplitudes, and then ensemble averaging, (see section 3.5). For convenience and brevity we will drop the time dependence of these voltages, and the ω dependence of their FT. From (V1(t)-V2(t)) we have;

$$FT\{(V1-V2)\} = FT\{V1\} - FT\{V2\} = \mathcal{V}1-\mathcal{V}2\,, \tag{7.2}$$

$$(\mathcal{V}1-\mathcal{V}2)(\mathcal{V}1-\mathcal{V}2)^{*} = \mathcal{V}1\mathcal{V}1^{*} + \mathcal{V}2\mathcal{V}2^{*} - \mathcal{V}1\mathcal{V}2^{*} - \mathcal{V}1^{*}\mathcal{V}2\,, \tag{7.3}$$

$$(\mathcal{V}1-\mathcal{V}2)(\mathcal{V}1-\mathcal{V}2)^{*} = \mathcal{V}1\mathcal{V}1^{*} + \mathcal{V}2\mathcal{V}2^{*} - \mathcal{V}1\mathcal{V}2^{*} - (\mathcal{V}1\mathcal{V}2^{*})^{*}\,, \tag{7.4}$$

$$(\mathcal{V}1-\mathcal{V}2)(\mathcal{V}1-\mathcal{V}2)^{*} = \mathcal{V}1\mathcal{V}1^{*} + \mathcal{V}2\mathcal{V}2^{*} - 2Re[\mathcal{V}1\mathcal{V}2^{*}]\,, \tag{7.5}$$

$$\langle(\mathcal{V}1-\mathcal{V}2)(\mathcal{V}1-\mathcal{V}2)^{*}\rangle = \langle\mathcal{V}1\mathcal{V}1^{*}\rangle + \langle\mathcal{V}2\mathcal{V}2^{*}\rangle - 2Re\langle\mathcal{V}1\mathcal{V}2^{*}\rangle\,, \tag{7.6}$$

$$\langle(\mathcal{V}1-\mathcal{V}2)(\mathcal{V}1-\mathcal{V}2)^{*}\rangle = S_{V1V1}(\omega) + S_{V2V2}(\omega) - 2Re[S_{V1V2}(\omega)]\,. \tag{7.7}$$

Similarly for (V1(t)+V2(t)) we obtain;

$$\langle(\mathcal{V}1+\mathcal{V}2)(\mathcal{V}1+\mathcal{V}2)^{*}\rangle = \langle\mathcal{V}1\mathcal{V}1^{*}\rangle + \langle\mathcal{V}2\mathcal{V}2^{*}\rangle + 2Re\langle\mathcal{V}1\mathcal{V}2^{*}\rangle\,, \tag{7.8}$$

$$\langle(\mathcal{V}1+\mathcal{V}2)(\mathcal{V}1+\mathcal{V}2)^{*}\rangle = S_{V1V1}(\omega) + S_{V2V2}(\omega) + 2Re[S_{V1V2}(\omega)]\,. \tag{7.9}$$

Here, $Re[S_{V1V2}(\omega)]$ represents the real part of $S_{V1V2}(\omega)$.

The noise voltage measurements on a single drain give $S_{V1V1}(\omega)$ and $S_{V2V2}(\omega)$. Since V1(t) and V2(t) are real the respective PSDs are real, and

furthermore $S_{V1V1}(\omega)\geq 0$ and $S_{V2V2}(\omega)\geq 0$ [42]. These two spectra are essentially identical, i.e. (V1)^2 and (V2)^2 for any device can not be distinguished. Since the devices are quite symmetric this is expected, otherwise a great disparity between (V1)^2 and (V2)^2 would make it advantageous to take the signal from one drain rather than the other. Thus, with $S_{V1V1}(\omega) = S_{V2V2}(\omega)$ we can rewrite equations (7.7) and (7.9) as;

$$\langle(\mathcal{V}1-\mathcal{V}2)(\mathcal{V}1-\mathcal{V}2)^*\rangle = 2S_{V1V1}(\omega) - 2\mathrm{Re}[S_{V1V2}(\omega)]\,, \tag{7.10}$$

$$\langle(\mathcal{V}1+\mathcal{V}2)(\mathcal{V}1+\mathcal{V}2)^*\rangle \doteq 2S_{V1V1}(\omega) + 2\mathrm{Re}[S_{V1V2}(\omega)]\,. \tag{7.11}$$

The left hand sides of equations (7.10) and (7.11), which represent the spectra (V1-V2)^2 and (V1+V2)^2 respectively, are measured experimentally. Since the variances of the differences [(V1-V2)^2-(V1)^2] and [(V1)^2-V1+V2)^2] are not too large we will assume that the differences are constant, (see Table 7.3). A constant difference on a log log plot implies that the left hand sides of equations (7.10) and (7.11) are related to $S_{V1V1}(\omega)$ by a multiplicative constant. The average differences between spectra and the resulting ratios $\mathrm{Re}[S_{V1V2}(\omega)]/S_{V1V1}(\omega)$ using equations (7.10) and (7.11) are listed in Table 7.3. Except for equation (7.11) as applied to the wide geometry, the ratios $\mathrm{Re}[S_{V1V2}(\omega)]/S_{V1V1}(\omega)$ are all about -1.0. The time average cross correlation of V1(t) and V2(t) can be obtained by inverse Fourier transforming the cross spectral density $S_{V1V2}(\omega)$, as claimed by the

Wiener-Khinchin theorem [34, 42]. Since the imaginary part of $S_{V1V2}(\omega)$ is lost, (see equations (7.4), (7.5)), the time average cross correlation can not be recovered using these measured spectra.

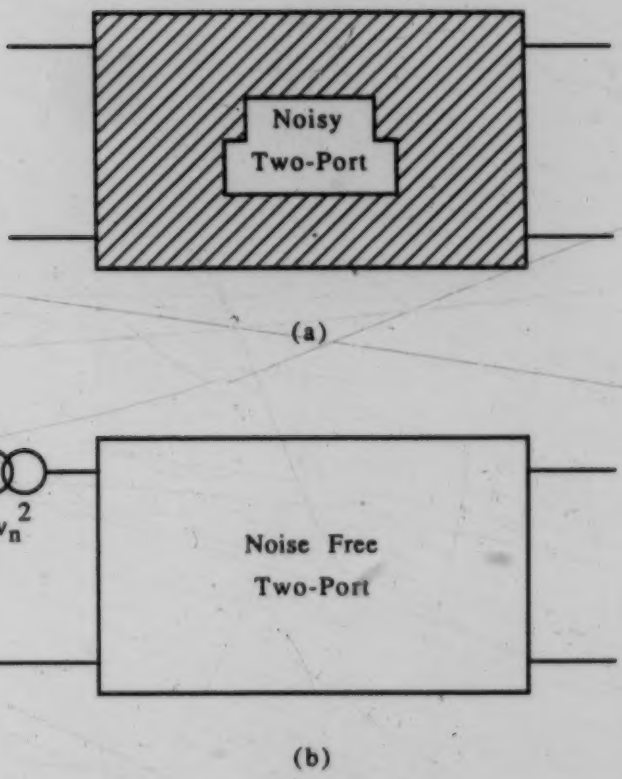

Fig. 7.1 Noisy two-port, (a). Equivalent representation with noise current and voltage generators referenced to the input, (b).

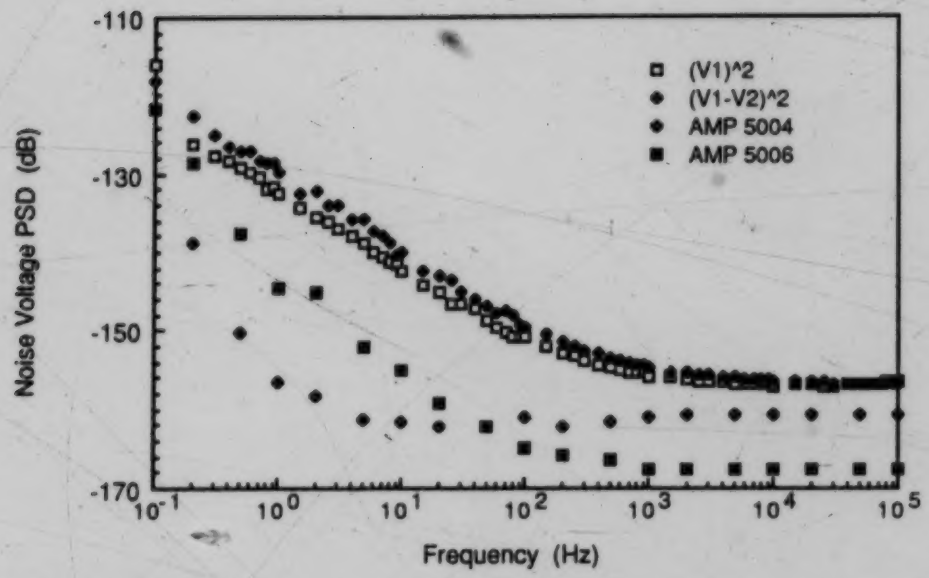

Fig. 7.2 The power spectral density of various noise voltages from the square MAGFET (W/L=100μm/100μm), operating in the MOS linear region. Device fabricated via Northern Telecom. Noise voltage PSDs of the measurement system using the different amplifiers are shown as well.

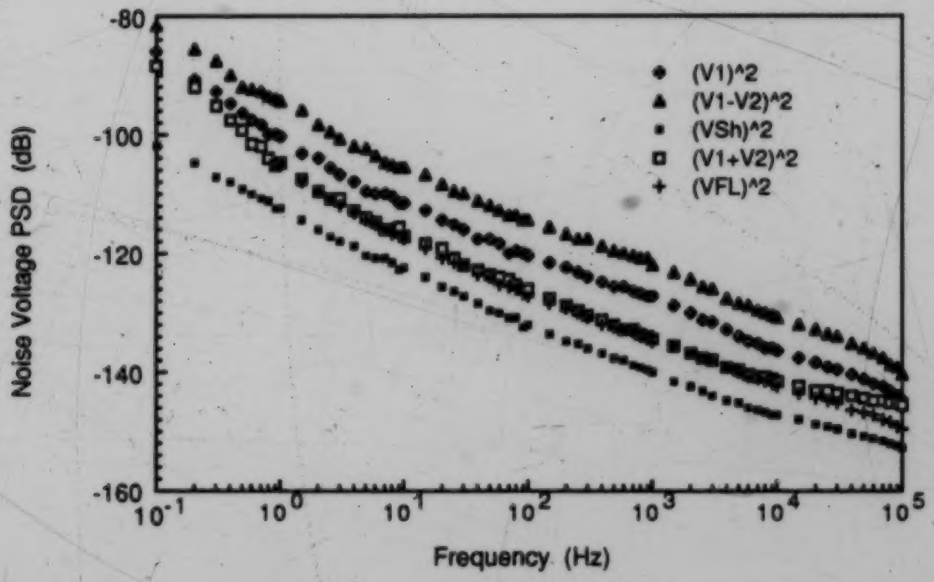

Fig. 7.3 The power spectral density of various noise voltages from the square MAGFET (W/L=100μm/100μm), operating in the MOS saturation region. Device fabricated via Northern Telecom.

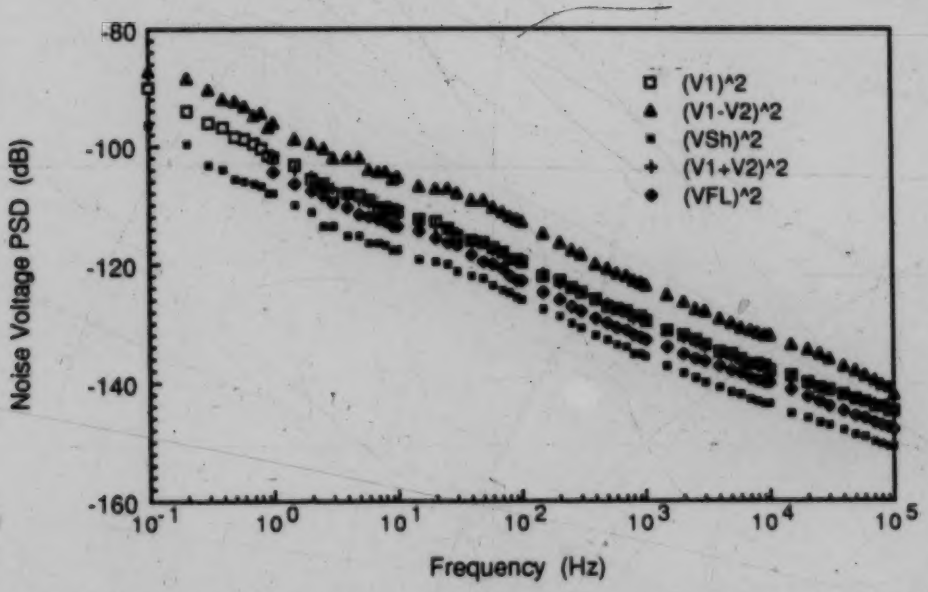

Fig. 7.4 As in Fig. 7.3, but for the wide MAGFET (W/L=100μm/25μm).

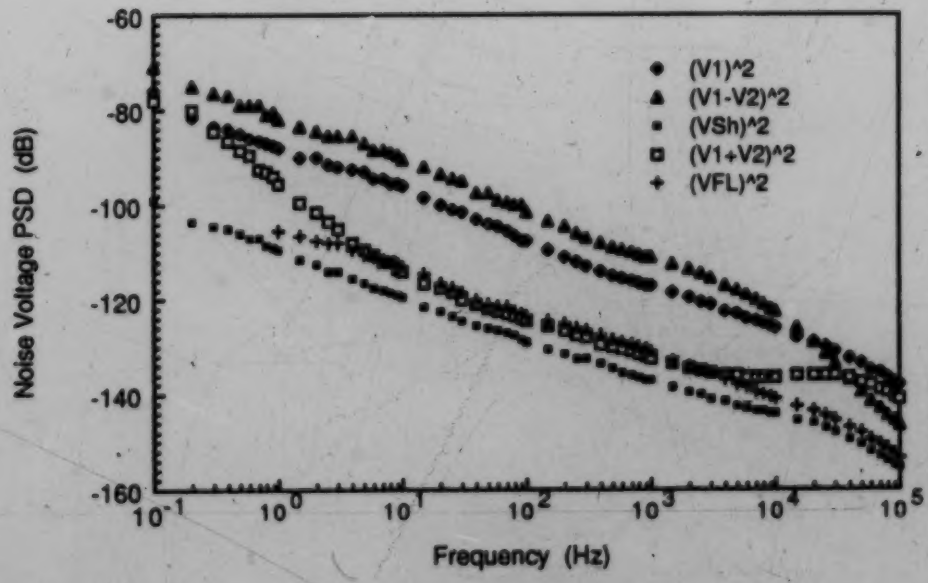

Fig. 7.5 As in Fig. 7.3, but for the long MAGFET (W/L=25μm/100μm).

Table 7.1 MAGFET geometry and corner frequency

MAGFET geometry W/L	100/100	100/25	25/100
Device thermal noise level x 10^-18 (V^2/Hz)	251	156	749
Measurement system thermal noise level x 10^-18 (V^2/Hz)	2	1	3
Thermal noise level of resistive elements x 10^-18 (V^2/Hz)	254	107	909
Total thermal noise level x 10^-18 (V^2/Hz)	505	264	1661
Corner frequency using total thermal noise level (kHz)	18.2	121	14.3
Corner frequency using device thermal noise level (kHz)	37.4	209	34.5

Table 7.2 MAGFET geometry and Signal to Noise Ratio

MAGFET geometry W/L		100/100	100/25	25/100
From a single drain	Signal (mV/T)	166	55.5	222
	RMS noise (μV)	.432	.335	1.38
	SNR x10^3 (1/T)	386	166	161
	Bmin (μT)	2.6	6.0	6.2
From between drains	Signal (mV/T)	333	111	444
	RMS noise (μV)	.813	.653	2.75
	SNR x10^3 (1/T)	410	170	162
	Bmin (μT)	2.4	5.9	6.2

Table 7.3 Average difference between spectra and the cross spectral density

Geometry W/L	100/100	100/25	25/100
Frequency range used for averaging. (Hz)	1 - 10k	1 - 10k	1 - 1k
Number of data points	45	45	34
Average of ((V1-V2)^2-(V1)^2) and standard deviation. (dB)	5.9 ±.4	6.0 ±.6	6.2 ±.4
Average of ((V1)^2-(V1+V2)^2) and standard deviation. (dB)	5.7 ±.8	0.1 ±.3	15.7 ±2.5
$Re[S_{V1V2}(\omega)]/S_{V1V1}(\omega)$ Using equation (7.10).	-.96 ±.18	-1.01 ±.27	-1.04 ±.27
$Re[S_{V1V2}(\omega)]/S_{V1V1}(\omega)$ Using equation (7.11).	-.87 ±.03	-.51 ±.04	-.99 ±.01

OUTLOOK AND CONCLUSIONS

The tests performed on the split drain MAGFETs and the VHDs have provided a considerable amount of information regarding their performance as magnetic field sensors. The results have been used to compare actual devices and their numerical models. For the MAGFET it was possible to construct a low frequency small signal circuit model. The attempts made here are by no means complete. More probing endeavors can certainly be initiated from them. Future efforts in modelling MAGFETs can avail themselves of the documented behaviour of sensitivity. In turn the results point to the potential of these devices as tools for process parameter evaluation. The MAGFET in particular can also be used to study magnetic phenomena in inversion layer, and noise in MOS devices. These are observations as a whole, the more specific ones follow.

For the MAGFET we find that the sensitivity in terms of relative current imbalance depends on geometry, channel type, bias point, and fabrication process. The dual drain MAGFET becomes more sensitive with decreasing channel width to length ratio. The three n-channel geometries tested, W/L= 4, W/L=1, W/L=.25, have the following typical sensitivities respectively, 1%, 4.5%, 5.5%. For W/L smaller than .25 the sensitivity is not expected to increase much more. Making W/L small by decreasing W to the limit imposed by design rules incurs problems. With a small width it becomes less likely that the drain sizes are equal or that the drain separation is centred, thus producing larger offsets. Although the dependence of the relative current imbalance for the two square geometries as a function of bias is

similar, it is evident that scaling does have an affect. For the smaller square MAGFET the dependence on V_{DS} and V_{GS} is more pronounced. Since the channel length of the 25 μm square MAGFET is smaller, the longitudinal electric field, relative size of the depletion region, and variation of mobile charge density along the channel length are greater. Some difference with respect to V_{DS} is then expected. Possible causes for the difference with V_{GS} are not as clear.

The averaging technique used to eliminate the offsets also eliminates any portion of the current imbalance dependent on B^2. Fortunately the total current changes very little for $|B| \leq 1$ T. This fact together with the virtually linear plots of δ versus B, even if the current imbalance is normalized to the total current at zero field, indicate that any portion of the current imbalance dependent on B^2 is quite small. For practical purposes the device response to $|B| \leq 1$ T can be considered linear.

One proposed method of increasing sensitivity is to have three drains rather than two. Provided that the current imbalance between the two exterior drains is normalized to the current flowing through the same two drains this is found to be true. However if the current imbalance is normalized to the sum of the current in all three drains the sensitivity decreases. The higher sensitivity of the triple drain MAGFET is more a matter of definition. Its actual current imbalance (I_1-I_2) is not expected to be better than a dual drain MAGFET of identical channel size.

A manner in which the MAGFET can be improved is by placing Hall contacts along the channel length. This produces a combined Hall plate and

split drain structure. If the device is not of minimum size this is easily managed, permitting the detection of magnetic field with Hall voltage and current imbalance simultaneously.

Sensitivity is noticeably affected by the operating voltages V_{GS}, V_{DS}, and V_{SB}. The sensitivity of each MAGFET increases with increasing V_{DS}. In the MOS linear region this could be due to the variation of mobile charge density along the channel length. In the MOS saturation region the emergence of the depletion region could be another contributing factor. A very consistent result is the peaking of δ with V_{GS}. This may be explained by Coulomb screening, however the value of gate voltage at which the peak occurs depends on the channel geometry, which does not seem consistent with this theory. For a fixed V_{GS} and V_{DS} the relative imbalance is not greatly affected by the source to substrate voltage. This is true for operation in the saturation region. The only means by which V_{SB} can adversely affect δ is by being large enough to place the device in the MOS linear region or turn the device off. By varying V_{SB} it is also found that the peaks in δ are coincident in terms of $(V_{GS}-V_T)$, whether the device is in the MOS linear or saturation region. This indicates that the sensitivity, and hence the Hall mobility, is dependent on the transverse electric field in the channel.

The difference in the sensitivities of the Microtel Pacific and the Northern Telecom MAGFETs indicate that the process is influential. The Northern Telecom n-channel MAGFETs have sensitivities about 10% greater than their Microtel counterparts. However only one batch run from each fabricator was used. This difference should not be construed as indicative of

the relative merits of these two processes. The p-channel MAGFETs show the greatest difference. The Northern Telecom p-channel MAGFETs register twice the sensitivity of the Microtel versions. This discrepancy definitely warrants further investigation. Although a larger number of samples would be required for a more conclusive statistical analysis, the number of samples used here should give a good indication. For any MAGFET geometry in either process the sensitivity as a function of bias varies marginally from the average. This is not too surprising since the MAGFET is basically dependent on carrier deflection in a MOSFET channel. This consistency of behaviour is a strong asset for qualifying it as a microelectronic sensor.

The VHD, by accident or design, is conveniently suited to detecting magnetic field with current and voltage imbalance simultaneously. Popovic visualized it as a deformed Hall plate. Its response V_H is essentially proportional to IB, just as for a rectangular Hall plate. The fact that it can detect fields parallel to the chip surface gives it a distinct advantage as a CMOS microelectronic sensor. The VHDs tested here are all realized in n-substrate. As a result currents can flow throughout the chip width and well beyond the area bounded by the contacts. If the VHD is realized in a p-well the current is constrained to flow in a much smaller region. For this reason, and the fact that holes are then the current carriers, such a VHD could possess sensitivities significantly different than those reported here.

Comparing the long, short, Popovic, and numerically modelled VHDs presents some difficulties. Depending on the desired signal, current or voltage imbalance, and the definition of sensitivity any one of these VHDs can be considered superior. Sensitivity for the VHD defined in terms of $(1/V)(\partial V_H/\partial B)$ or $(1/I)(\partial I_H/\partial B)$ has the property of being practically

independent of biasing. A definition like $(1/I)(\partial V_H/\partial B)$ favours VHDs with a higher resistance between contacts. Since these devices consume energy in order to detect magnetic field a condition is imposed on the absolute sensitivities $\partial V_H/\partial B$ and $\partial I_H/\partial B$. The condition is that the power consumption, at which the absolute sensitivity is computed, must be the same for all the devices compared. This definition of sensitivity is not proposed to be definitive in comparing devices. It is merely another possible means of comparison, based on the notion that the devices have the same amount of energy to work with.

The method described to measure Hall and drift mobility is very straightforward and plausible. The derived values of electron scattering factor, $r_n>1$, from both the Northern Telecom and Microtel Pacific devices are all quite reasonable. However, the confidence in this result is overshadowed by the uncertainty in the exact values of C'_{ox}, K, and W/L. The figure for C'_{ox} is a quoted not measured value. The W/L ratio disregards the presence of the drain separation. The geometric factors K are obtained via numerical modelling with no other corroboration. Modifications to the W/L ratio can be obtained via numerical modelling. A means of verifying the values of K and adjusting the W/L ratio is to have appropriate structures on the chip. This requires equal sized single and dual drain MOSFETs for the latter, and long MOS Hall plates for the former. In all the devices tested, except the wide MAGFET, the electron scattering factor is practically constant for strong inversion. For the wide MAGFET r_n apparently increases with V_{GS}. The immediate cause of this effect seems to be the drift mobility degrading too

quickly with V_{GS}.

A low frequency equivalent circuit representation of the dual drain MAGFET in saturation was developed. Using the sensitivity results and the measured device output characteristics the circuit model is comprised of three resistive elements and a magnetic field dependent ideal current source. For $|B| \leq .01$ T, or $|B| > .1$ T and load resistances that are quite small compared to the equivalent circuit elements, hand calculations can give fairly accurate results. A more comprehensive model for circuit simulation programs should account for the resistive elements changing with terminal voltages, from the saturation through to the linear region. Another possible requirement may be the inclusion of magneto-resistance effects.

The results from the noise measurements on the dual drain MAGFETs have both clarified and raised a few questions. For the large square device in the saturation region, the noise power from a single drain or between drains is indistinguishable from the zero field case or B=.27 T. The signal to noise ratio is essentially the same whether the signal is from a single drain or from between drains. This applies to each geometry tested in the saturation region, with SNR defined as the ratio of the signal level to the RMS noise level. Of the three geometries tested the square MAGFET has the lowest detectable field. However, this may be by virtue of its larger area. If the wide and long devices are scaled to have the same channel area as the square, their B_{min} could be as low as that of the square MAGFET.

The most surprising result, which certainly requires further investigation, is the approximately 6 dB difference between the power spectra for the noise voltage from between drains and from a single drain.

This seems to be the rule for all the devices in saturation, where the spectra are all approximately 1/f. In the linear region test for the square MAGFET a smaller difference is noticeable, however the noise levels are much lower and the true difference may be obscured by noise from the measurement system. The spectra in this instance are 1/f for the lower frequencies and flat for the higher frequencies. Perhaps this difference is peculiar to 1/f noise. The explanation of this phenomenon could help in identifying or understanding noise mechanisms in MOS devices.

From the spectra measured, and their average relative difference, the real part of the power cross spectral density of the two drain voltages, $S_{V1V2}(\omega)$ was estimated. This was expressed relative to the power spectral density from a single drain, $S_{V1V1}(\omega) \approx S_{V2V2}(\omega)$, which is a positive real quantity. For the NMOS dual drain geometries tested in the MOS saturation region the result is that $Re[S_{V1V2}(\omega)] \propto -S_{V1V1}(\omega)$, with the proportionality constant being near unity. All the spectra used in this calculation have a 1/f dependence.

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APPENDIX A

ERROR ANALYSIS

A.1 Error Calculations for the MAGFET

In this and the following sections on error analysis we estimate the error in the quantities reported. The errors considered are solely from instrument accuracy and resolution, and their propagation through arithmetic calculations.

The semiconductor parameter analyser can measure currents to a resolution of 4 digits to at best 50 fA. Thus from the instruments resolving capability a measured current I has an error of ±.0005I or ±.05%. The resulting error in the difference between two measured currents is;

$$I_1 \pm (.0005I_1) - I_2 \pm (.0005I_2) = I_1 - I_2 \pm (.0005(I_1 + I_2)) \quad (A.1)$$

$$(I_1 + I_2)/(I_1 - I_2) = 1/\delta \quad (A.2)$$

$$\therefore I_1 - I_2 \pm (.05/\delta)\ \%. \quad (A.3)$$

The error in the current imbalance is inversely proportional to the relative imbalance. The error in the sum of the two currents is;

$$I_1 \pm (.0005I_1) + I_2 \pm (.0005I_2) = I_1 + I_2 \pm (.0005(I_1 + I_2)) \quad (A.4)$$

$$I_1 \pm (.0005I_1) + I_2 \pm (.0005I_2) = I_1 + I_2 \pm (.05)\%. \qquad (A.5)$$

The error in the relative imbalance δ, from the error in measuring the currents, is the sum of the relative errors in equations (A.3) and (A.5);

$$\delta = (I_1 - I_2)/(I_1 + I_2) \pm (.05(1 + 1/\delta))\%. \qquad (A.6)$$

It must be remembered that this relative error is for the worst case resolution. For the best case resolution the factor .05 in equation (A.6) must be changed to .005.

The contribution to the relative error in δ from the uncertainty of knowing the exact value of magnetic field B is $\delta^{-1}(\partial\delta/\partial B)\delta B$. For all the devices tested $\partial\delta/\partial B$ is effectively a constant, (ie. a linear response). The magnitude of this quantity being δ at one tesla, in units of 1/T. The error in measuring the magnetic field is the sum of the accuracy of the probe, gaussmeter, and its calibration. These are about .5% each. As was mentioned in the procedure there is an additional 1% error on the probe, since the magnitude of the reading is not the same when it aligned parallel and anti-parallel to the field. Aside from measuring the value of the magnetic field, there is the task of aligning the chip parallel or perpendicular to the field direction. The field strength along a line making an angle θ with the direction of the magnetic varies as $\sin(\theta)$. As a result an error in angular orientation of as much as 5 degrees will only change the magnitude of the field by less than 0.5%. Thus the magnetic field is measured with an accuracy of about ± 3.0%,

hence $\delta B = 0.03B$. If offsets are small, then $\delta/B \approx \partial\delta/\partial B$. The result is a contribution of 3.0% to the error term in equation (A.6).

$$\delta \pm (.05(1+1/\delta) + 3.0)\%. \qquad (A.7)$$

The percentage error for a few values of δ are shown in Table A.1.

Table A.1 Relative current imbalance δ and error

δ (%)	0.5	1.0	2.0	3.0	4.0	5.0	6.0	7.0
Relative Error (%)	13.1	8.1	5.6	4.7	4.3	4.1	3.6	3.6

In some of the graphs the plotted relative imbalance is actually;

$$(\delta(B) - \delta(-B))/2. \qquad (A.8)$$

If the current imbalance at zero field is small enough then for $\delta(B)$ positive $\delta(-B)$ is negative. The expression (A.8) becomes;

$$(\delta(B) + |\delta(-B)|)/2. \qquad (A.9)$$

The expression for the relative error in δ is of the form $(a+c/\delta)\%$, with a=3.05

and c=.05. Using this to calculate the error in (A.9) we have;

$$(\delta(B) + |\delta(-B)|)/2 \pm [\delta(B)(a + c/\delta(B)) + |\delta(-B)|\,(a + c/|\delta(-B)|)]/2, \qquad (A.10)$$

$$(\delta(B) + |\delta(-B)|)/2 \pm [a((\delta(B) + |\delta(-B)|)/2) + c] \qquad (A.11)$$

$$\delta \pm (a + c/\delta)\% \qquad (A.12)$$

Expression (A.12) is obtained from (A.11) by substituting δ for $(\delta(B)+|\delta(-B)|)/2$, and dividing by δ to revert to the relative error form. Thus (A.12) is identical to (A.7). If the current imbalance at zero field is large enough so that for $\delta(B)$ positive $\delta(-B)$ is positive as well the resulting relative error will be different than in (A.12). The term $(\delta(B)-\delta(-B))/2$ can not be written as in (A.9). Repeating the previous steps the relative error in this case is;

$$\delta \pm [a(\delta(B) + \delta(-B))/(\delta(B) - \delta(-B)) + c/\delta]\,\%. \qquad (A.13)$$

If $\delta(B)$ and $\delta(-B)$ are both large and positive the term 'a' is multiplied by a factor greater than unity, making the relative error larger than in (A.7).

The relative current imbalance of the MAGFET is also a function of applied voltages such as V_{GS} and V_{DS}. The contribution to the relative error in δ from a variable voltage V is, $\delta^{-1}(\partial\delta/\partial V)\Delta V$. The accuracy that voltages can be measured or set to is approximately 0.2%. Voltage resolution is better than 1 part in 2000 or 1 mV, whichever is greatest. Since these biasing voltages are not normalized to any other measured or set voltage there total error is

the sum of the uncertainty in the accuracy and the resolution. Unfortunately $\partial\delta/\partial V$ is not constant for V being any of the biasing voltages. In general the quantity $\delta^{-1}(\partial\delta/\partial V)$ is less than 5. The error in an applied voltage of 0.1 V is 1.2 mV. The product of these two figures results in a 6% relative error in δ. This is a rather extreme result. For voltage levels greater than 1.0 V $\delta^{-1}(\partial\delta/\partial V)$ is usually less than .5 V^{-1}, with the result that the relative error is at most about .5%. This error for various values of voltage and $\delta^{-1}(\partial\delta/\partial V)$ is shown in Table A.2. Thus for the dual drain MAGFET with the relative imbalance plotted as a function of V_{DS}, and V_{GS} as an additional variable, we would have to add this error to the relative error in Table A.1.

A.2 Error Calculations for the VHD

For the VHD there are three quantities plotted as a function of magnetic field, the relative current imbalance, the Hall voltage, and the Hall voltage referenced to the voltage at the centre terminal. The experimental error in each case will be assessed.

The error in the relative imbalance from the resolving power of the analyser is the same as given in equation (A.6). Using the same reasoning as in section A.1 the error in the magnetic field is again 3.0%. The contribution to the error from $(\partial\delta/\partial I)\Delta I$ is difficult to determine since the jumps in current are quite large. However, to get an idea of the magnitude of this error we can use the worst case variation of δ with I, which usually occurs at the lowest total current level. Using the short VHD for example, we say that $(\delta(100\mu A)-\delta(10\mu A))/(100\mu A-10\mu A)=(\partial\delta/\partial I)$ at the midpoint of the two current

levels, 55μA-50μA. The error in setting the total current level is ±.005I=ΔI. The resulting errors are ±.0002 for the short VHD, and ±.0001 for the long VHD. These errors are for δ not expressed as a percentage.

In measuring the Hall voltage the voltage monitors of the analyser were used. They have an accuracy of .5% with a resolution of .1mV. The magnitude of the voltage at the device Hall probes increases with increasing current. Consequently the errors in measuring and subtracting the two Hall probe voltages are ±.1 mV, ±.4 mV, ±4 mV, for the short VHD, from the lowest to highest total current level. Likewise for the long VHD they are ±.1 mV, ±.8 mV, ±7 mV. From the graphs of V_H versus B, and neglecting the offsets we notice that the Hall voltage can be expressed as V_H=cIB, where c is a constant. Thus we have $(\partial V_H/\partial I)$=cB. As before ΔI= ±.005I. For either VHD we obtain the result that $(\partial V_H/\partial I)\Delta I = \pm(.005)V_H$.

The error in calculating (V_H/V) is the sum of the relative error in each voltage. The error in measuring V is ±.5 mV. Since V increases with the applied current its relative error decreases. The relative error in V_H is simply the error in measuring and subtracting the two Hall probe voltages divided by V_H. From the graphs it can be seen that (V_H/V) is a weak function of total current. Going through the same procedure as mentioned for the relative current imbalance, the term $(\partial(V_H/V)/\partial I)\Delta I$ is quite small compared to the other errors and is therefore neglected. The error then in (V_H/V) is $\pm(.005+.025(V_H/V))$, $\pm(.002+.0025(V_H/V))$, $\pm(.002+.00025(V_H/V))$, for the

short VHD, from the lowest total current level to the highest. In the same manner we have $\pm(.0025+.0125(V_H/V))$, $\pm(.002+.0013(V_H/V))$, $\pm(.0018+.0003(V_H/V))$, for the long VHD. Again in these error estimates (V_H/V) is not expressed as a percentage.

A.3 Error Estimates For Mobility

In determining the drift mobility the slope of the I_D versus V_D curves was taken. This was calculated by way of $[I_D(V_D=.1)-I_D(V_D=0)]/(0.1)$. The error in this expression from the instrument accuracy and worst case resolution in about 2.2%. Since $\partial I_D/\partial V_D$ depends of V_G the uncertainty in V_G introduces error. Using the functional dependence on V_G obtained by taking the partial derivative of equation (3.3) with respect to V_D, this error is less than .25% for $V_G>1.0$ V. Thus from the measurement alone there is about 2.5% error in the drift mobility.

The calculation of drift mobility also hinges on knowledge of C'_{ox} and the ratio W/L. The value of C'_{ox} is certainly questionable, but for sake of continuing this analysis we will assume it has an error of ±10%. The uncertainty in W/L comes from knowing the actual values of W and L, and of course if the ratio W/L is applicable in equation (3.3) because of the drain separation. If the process can achieve various dimensions within a margin of ±.5 μm, then neglecting lateral diffusions, the error in W/L is 1%, 2.5%, and 2.5% for the square, wide, and long MAGFETs respectively. Thus the accuracy

of the drift mobility could be as much as ±15 %.

The Hall mobility measurement is based on the relative current imbalance. The error in the relative imbalance is the same as outlined in the first section of this appendix. Thus the error in the Hall mobility of the wide geometry is about 9% while for the square and long geometry it is about 5%. If K is accurate to within ±10%, the uncertainty in r can be quite large. For the wide MAGFET with a relative imbalance of 1%, the figures assumed here give an accuracy of around ±35%.

A.4 Noise Measurement Errors

The accuracy of each noise voltage power spectrum is estimated at ±0.7 dB, .2 dB from the spectrum analyser, and .5 dB from the amplifier gain. The resolution is about .02 dB, .01 dB apiece, from the spectrum analyser and amplifier gain. These figures only account for the measurement equipment accuracy and resolution. The other main source of error is the fact that the noise voltage is a random signal. The PSD value at each frequency varies from reading to reading. Any recorded PSD value is the average of a number of readings. The number of averages is a compromise between time and the fluctuation in the power spectrum. The spectra have fluctuations of about ±.1, ±.2 dB, ±.5 dB, and ±1 dB, for 5000, 2000, 300, and 100 averaged readings respectively. These are the only figures that can be provided as the variance in the PSD at each frequency point was not investigated. With fluctuations of this magnitude the final recorded values are rounded off to the nearest tenth of a decibel.

Table A.2 Relative error in δ from an applied voltage

		$(1/\delta)(\partial\delta/\partial V)$ x Error (%)		
V (Volts)	ΔV (mV)	$(1/\delta)(\partial\delta/\partial V)$= (1/Volts)		
		2	1	.5
.005	1.0	.2	.1	.05
.01	1.0	.2	.1	.05
.02	1.0	.2	.1	.05
.05	1.0	.2	.1	.05
.1	1.2	.24	.12	.06
.2	1.4	.28	.14	.07
.5	2.0	.4	.2	.10
1	3.0	.6	.3	.15
2	5.0	1.0	.5	.25
3	7.0	1.4	.7	.35
4	9.0	1.8	.9	.45
5	11.3	2.3	1.1	.55

APPENDIX B

RELATIVE IMBALANCE AND OFFSETS

To calculate the relative imbalance at a given field the following expression was used;

$$\delta^{*}(B) = (I_1(B) - I_2(B))/(I_1(B) + I_2(B)). \qquad (B.1)$$

If the denominator of this expression were the sum of currents at B=0 T then a plot of $\delta(B)$ versus B could reveal magneto-resistance effects. To avoid such effects devices are operated at a constant current. This is quite impractical for the MAGFET devices. Establishing operating points in terms of constant applied voltages is much easier, particularly in the MOS saturation region. Furthermore when investigating $\delta(B)$ as a function of operating point at a fixed value of B equation (B.1) is meaningful provided that $I_1(B=0)=I_2(B=0)$. This condition is rarely satisfied. To correct for this fact the zero field current imbalance, also called the offset, must be subtracted from the numerator;

$$I(B) = I_1(B) + I_2(B), \qquad (B.2)$$

$$\Delta I_0 = I_1(0) - I_2(0), \qquad (B.3)$$

$$\delta(B) = (I_1(B) - I_2(B) - \Delta I_0)/ I(B) . \qquad (B.4)$$

Again, if the denominator of (B.4) were the sum of currents at zero field then magneto-resistance effects could be observed.

In this work the plots of $\delta(B)$ versus operating point do not use (B.4) above. Instead the following expression is used to determine the plotted $\delta(B)$;

$$\delta(B) = (\delta^*(B) - \delta^*(-B))/ 2 . \qquad (B.5)$$

Equation (B.5) is used as a means of eliminating the zero field offsets. It is successful to this end depending on the functional dependence of the current imbalance on the magnetic field.

To illustrate what the relative imbalance produced by (B.5) is we make the following assumptions;

$$\Delta I(B) = I_1(B) - I_2(B) = I(a_0 + a_1 B + a_2 B^2) , \qquad (B.6)$$

$$I(B) = I_1(B) + I_2(B) = I(1 + c_1 B + c_2 B^2) , \qquad (B.7)$$

$$I = I_1(0) + I_2(0). \qquad (B.8)$$

The current imbalance and the total device current are expressed as a product of the total current at zero field and a quadratic function in B. The term a_0 is the relative current imbalance at zero field. The terms a_1 and a_2 account for the change in current imbalance with magnetic field. The terms c_1 and c_2 account for the change in the total current with magnetic field.

From some of the measurements we know that the total current decreases slightly whether B is +1 T or -1 T, and that the decrease is about the same for either value of B. Thus c_2 is small, approximately .01, and $c_1<c_2$. The plots of relative imbalance versus B indicate that the devices are quite linear. This is true for $\Delta I(B)$ normalized to I(B) or I(0), hence $a_2<a_1$. Using (B.6) and (B.7) in the right hand side of (B.5) and paying attention to the sign of B we obtain;

$$((a_0+a_1B+a_2B^2)/(1+c_1B+c_2B^2) - (a_0-a_1B+a_2B^2)/(1-c_1B+c_2B^2))/2 . \qquad (B.9)$$

Making the denominator in (B.9) $(1+c_1B+c_2B^2)(1-c_1B+c_2B^2)\approx(1+2c_2B^2)$, and performing the algebra we obtain;

$$a_1B(1+c_2B^2)/(1+2c_2B^2) - (a_0+a_2B^2)c_1B/(1+2c_2B^2) . \qquad (B.10)$$

Assuming that $2c_2B^2<1$ and that $(1+2c_2B^2)\approx1$ in the second term of (B.10) we have;

$$\delta(B) = a_1B(1-c_2B^2) - (a_0+a_2B^2)c_1B , \qquad (B.11)$$

$$\delta(B) = a_1B - a_1c_2B^2 - a_0c_1B - a_2c_1B^3 . \qquad (B.12)$$

From (B.12) we can see the effect of averaging the relative imbalance via (B.5) with B=1 T. Since c_2 is non zero the second term of (B.12) is about 1% of

a_1. If c_1 is zero then the third term is zero, and the zero field imbalance is eliminated. Note that $c_1=0$ also eliminates the non linear portion of the current imbalance a_2. The indications are that c_1 may be non zero, but quite small. Thus the zero field offset can produce an error in $\delta(B)$ if $a_0 c_1$ approaches a_1. From the comparison of current imbalance at +1 T and -1 T an estimate of c_1 is .001, thus for relative offsets at zero field as great as $10a_1$ only an additional 1% error in $\delta(B)$ would be incurred.

APPENDIX C

MAGFET CHARACTERISTICS

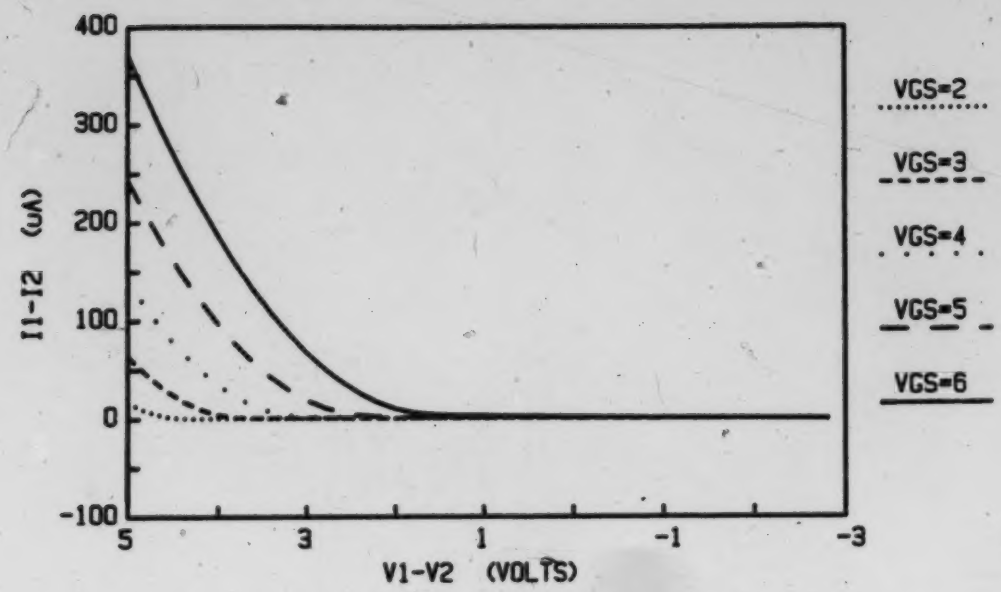

Fig. C1 Drain current difference as a function of drain voltage difference at various operating points, of the square dual drain MAGFET (W/L=100μm/100μm), fabricated via Northern Telecom. (I1-I2)=(I_{D1}-I_{D2}), (V1-V2)=(V_{D1}-V_{D2}).

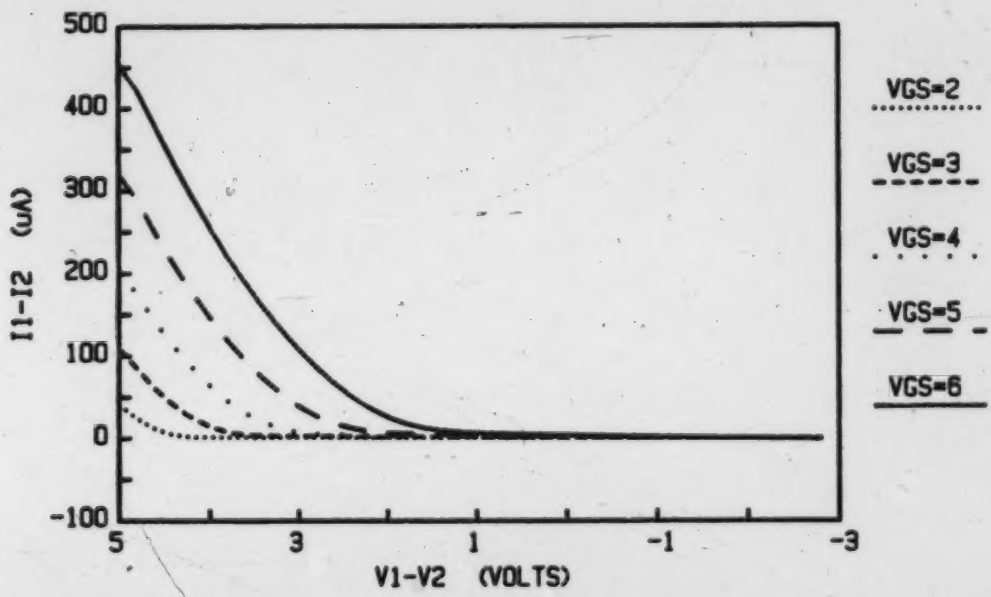

Fig. C2 As in Fig. C1, but for the square MAGFET (W/L=25μm/25μm).

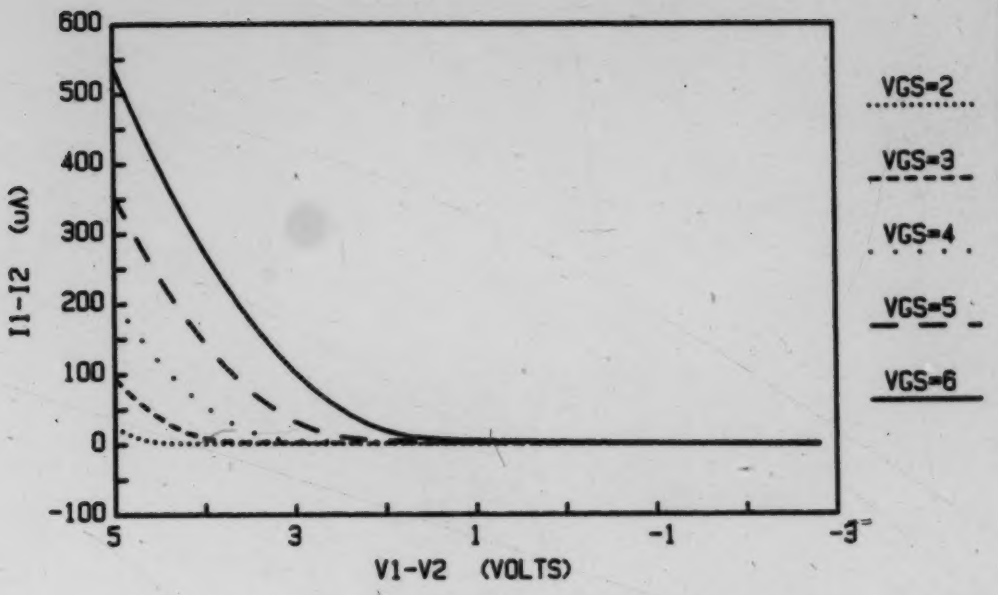

Fig. C3 As in Fig. C1, but for the wide MAGFET (W/L=100μm/25μm).

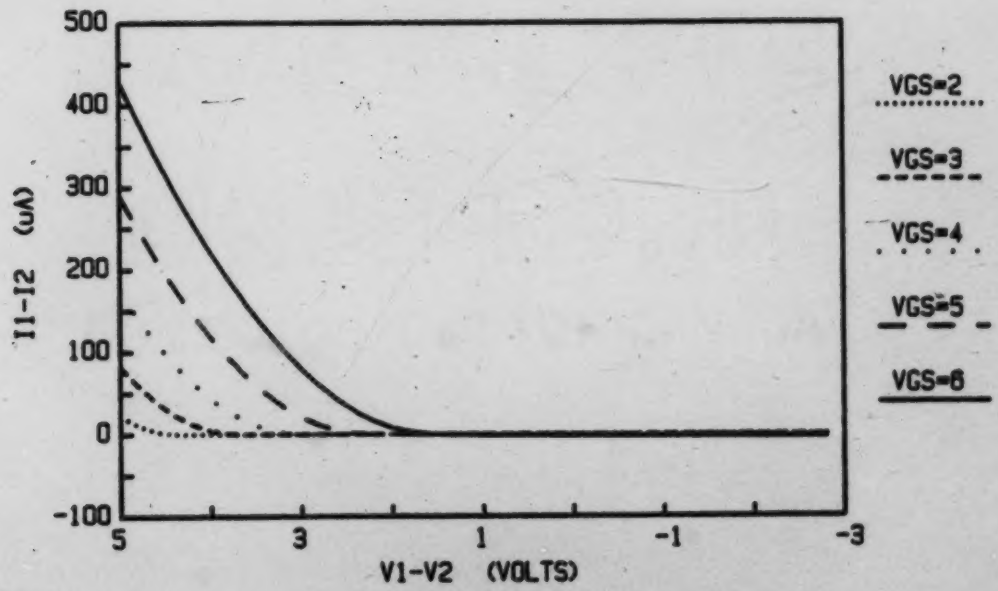

Fig. C4 As in Fig. C1, but for the long MAGFET (W/L=25μm/100μm).

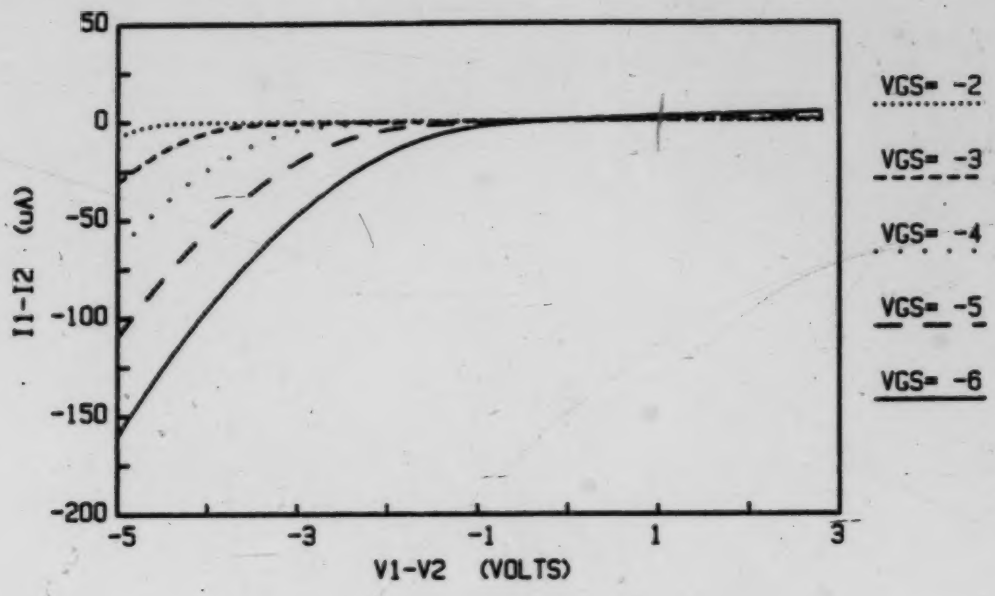

Fig. C5 As in Fig. C1, but for the PMOS MAGFET (W/L=75μm/25μm).

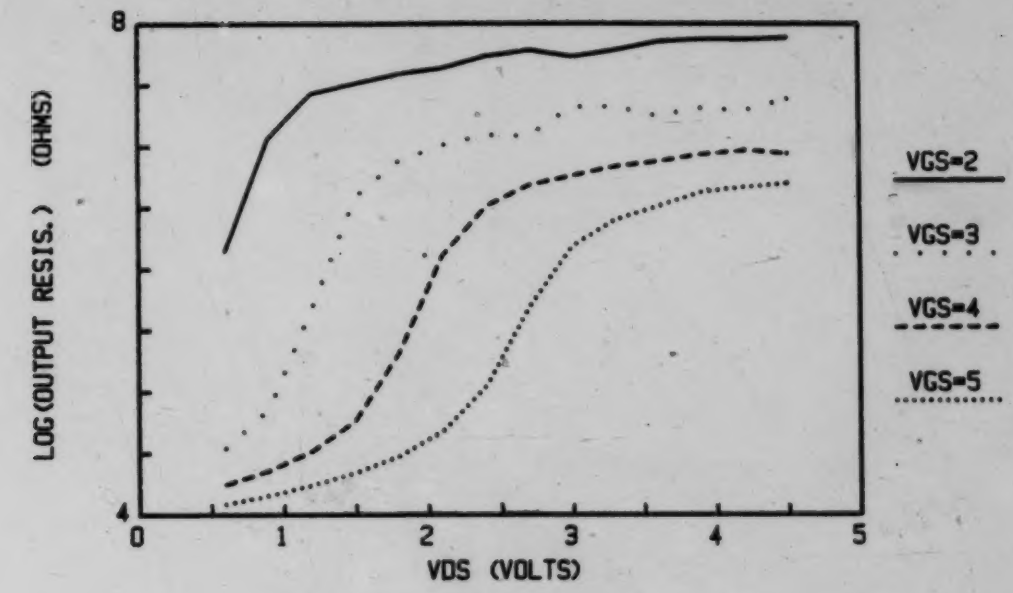

Fig. C6 Log_{10} of the incremental output resistance as a function of operating point, of the square dual drain MAGFET (W/L=100μm/100μm) with drains shorted, fabricated via Northern Telecom.

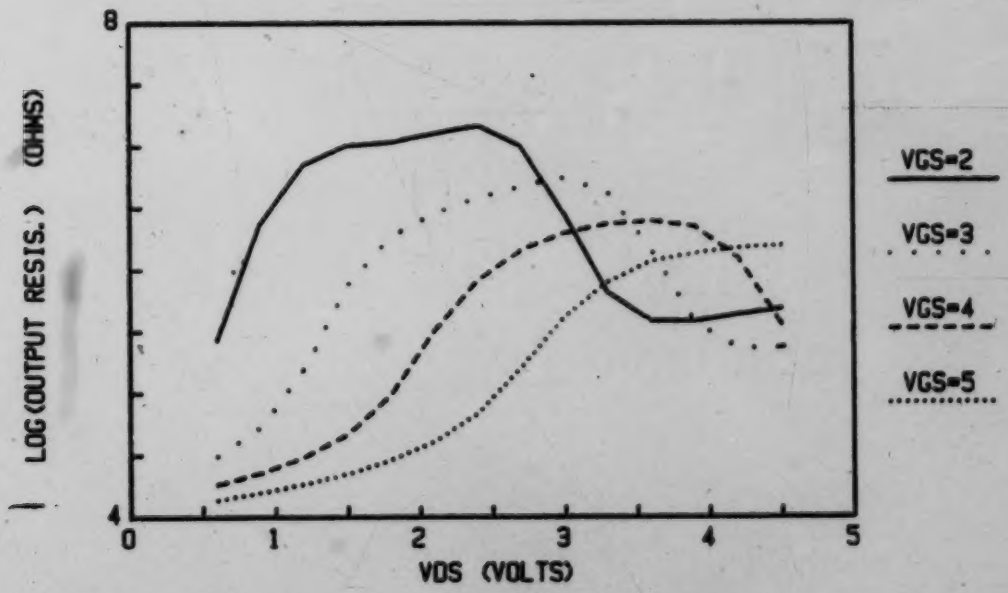

Fig. C7 As in Fig. C6, but for the square MAGFET (W/L=25μm/25μm).

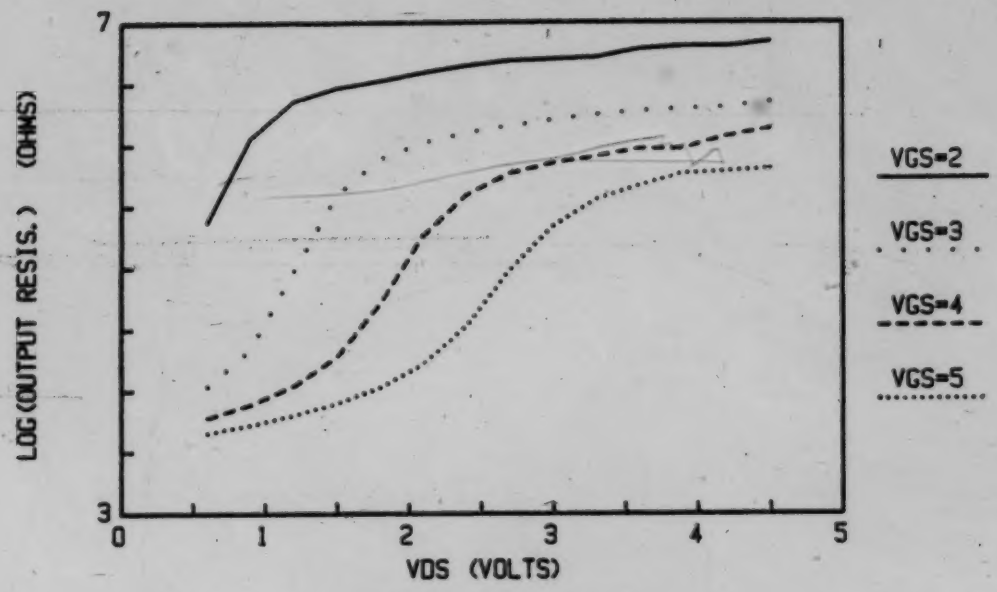

Fig. C8 As in Fig. C6, but for the wide MAGFET (W/L=100μm/25μm).

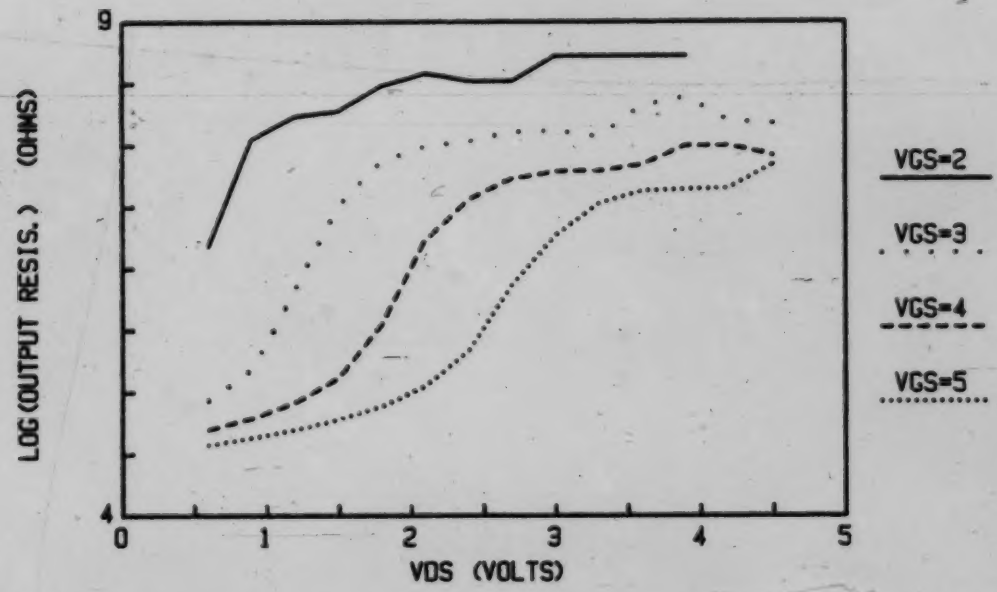

Fig. C9 As in Fig. C6, but for the long MAGFET (W/L=25μm/100μm).

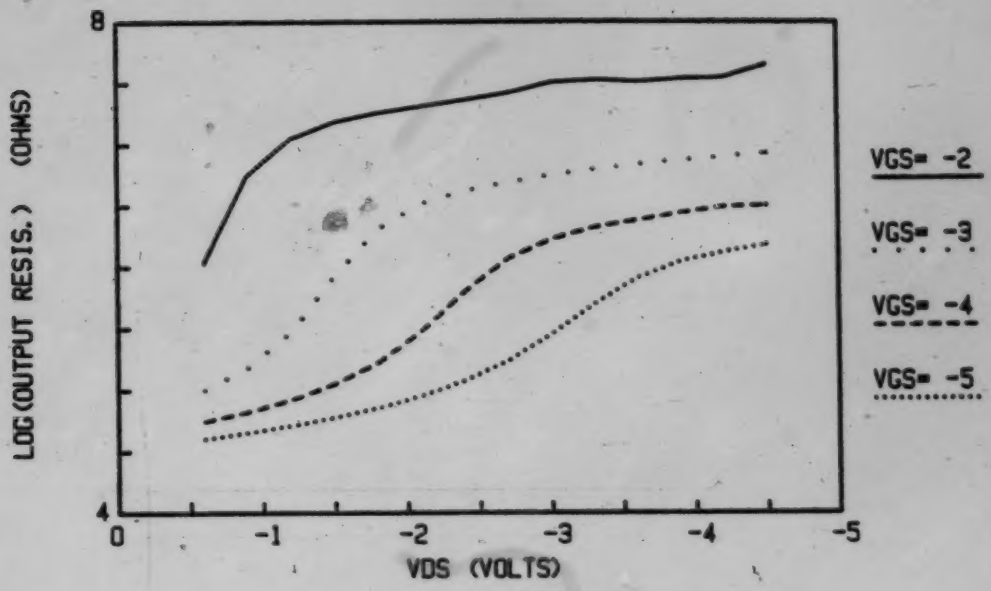

Fig. C10 As in Fig. C6, but for the PMOS MAGFET (W/L=75μm/25μm).

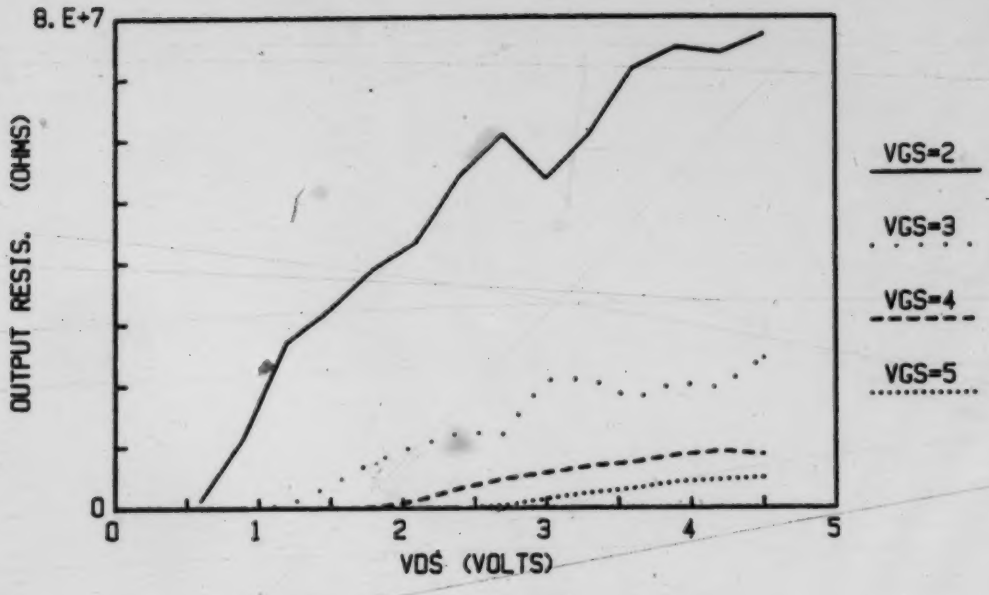

Fig. C11 Incremental output resistance as a function of operating point, of the square dual drain MAGFET (W/L=100μm/100μm) with drains shorted, fabricated via Northern Telecom.

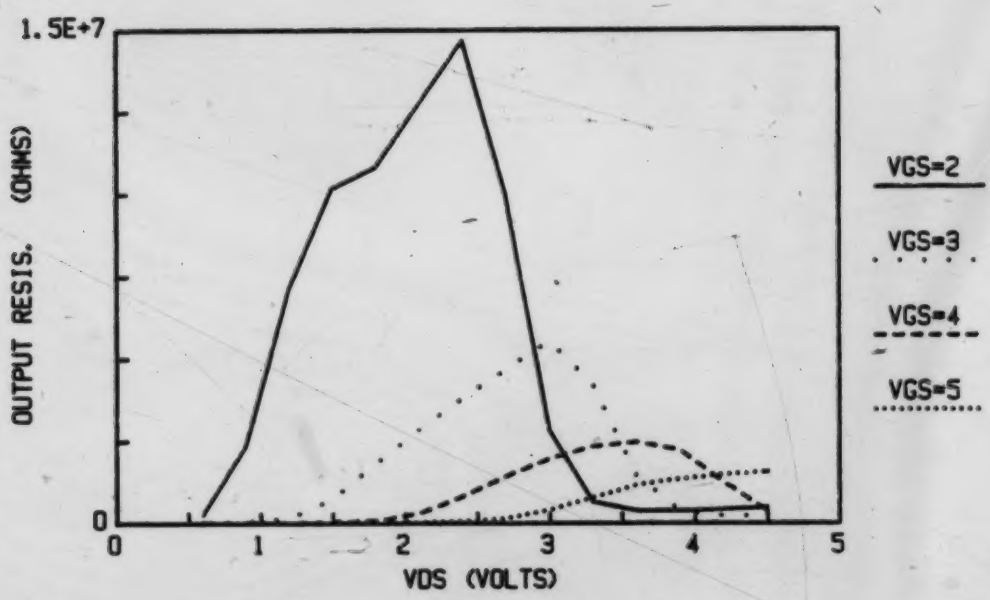

Fig. C12 As in Fig. C11, but for the square MAGFET (W/ =25μm/25μm).

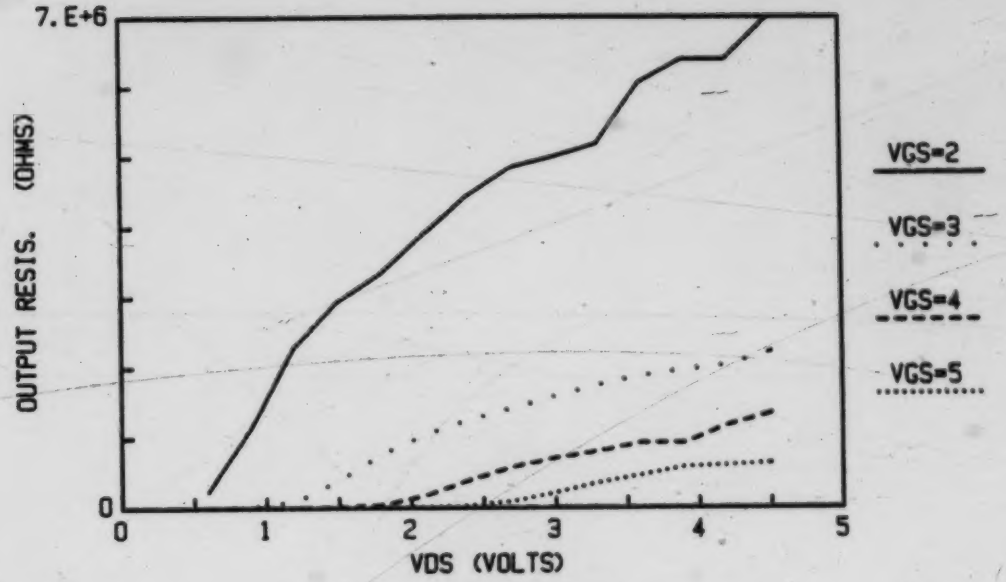

Fig. C13 As in Fig. C11, but for the wide MAGFET (W/L=100μm/25μm).

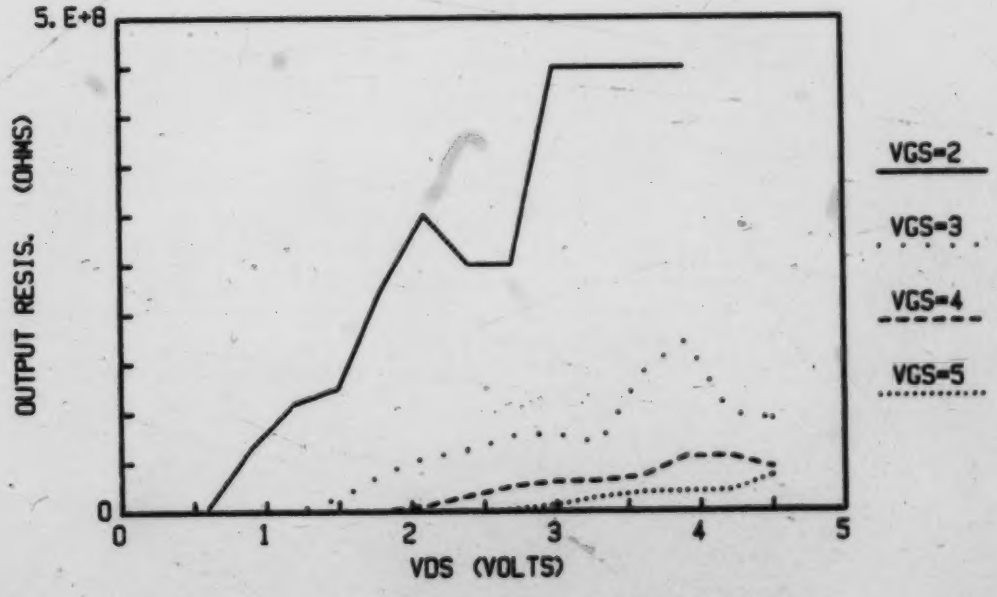

Fig. C14 As in Fig. C11, but for the long MAGFET (W/L=25μm/100μm).

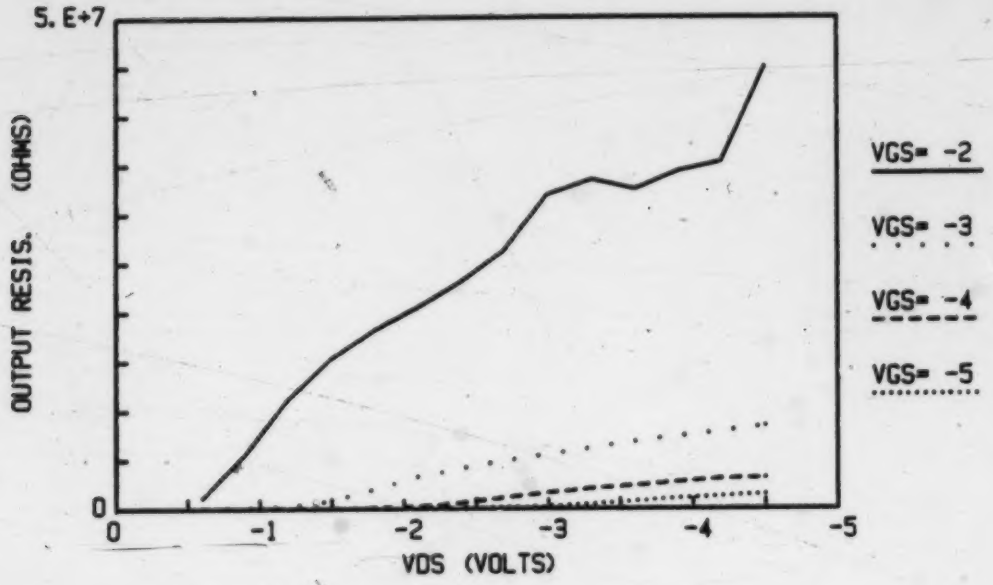

Fig. C15 As in Fig. C11, but for the PMOS MAGFET (W/ =75μm/25μm).

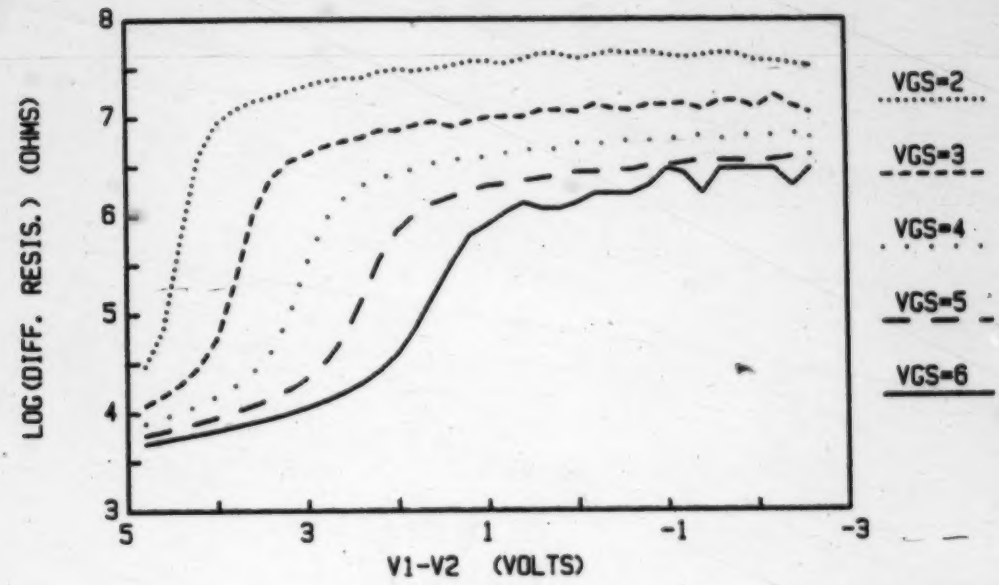

Fig. C16 Log_{10} of the incremental resistance between drains as a function of the drain voltage difference at various values of V_{GS}, of the square dual drain MAGFET (W/L =100μm/100μm), fabricated via Northern Telecom. (V1-V2)=(V_{D1}-V_{D2}).

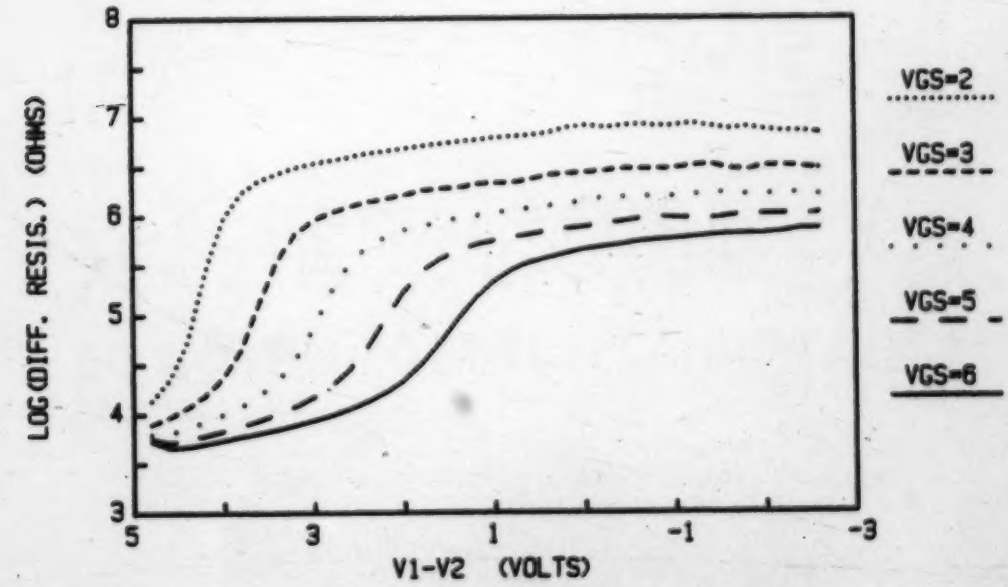

Fig. C17 As in Fig. C16, but for the square MAGFET (W/L=25μm/25μm).

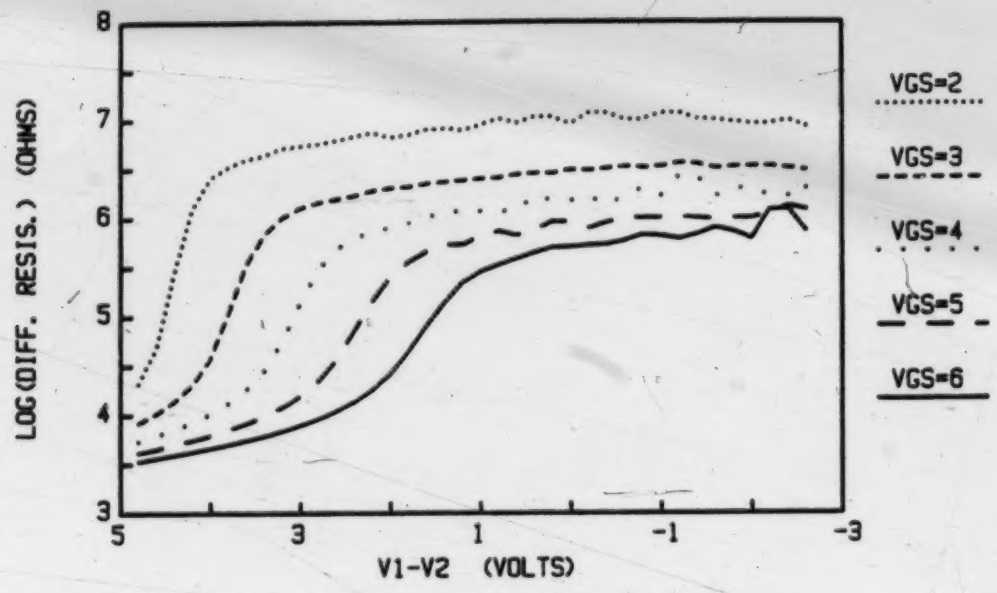

Fig. C18 As in Fig. C16, but for the wide MAGFET (W/L=100μm/25μm).

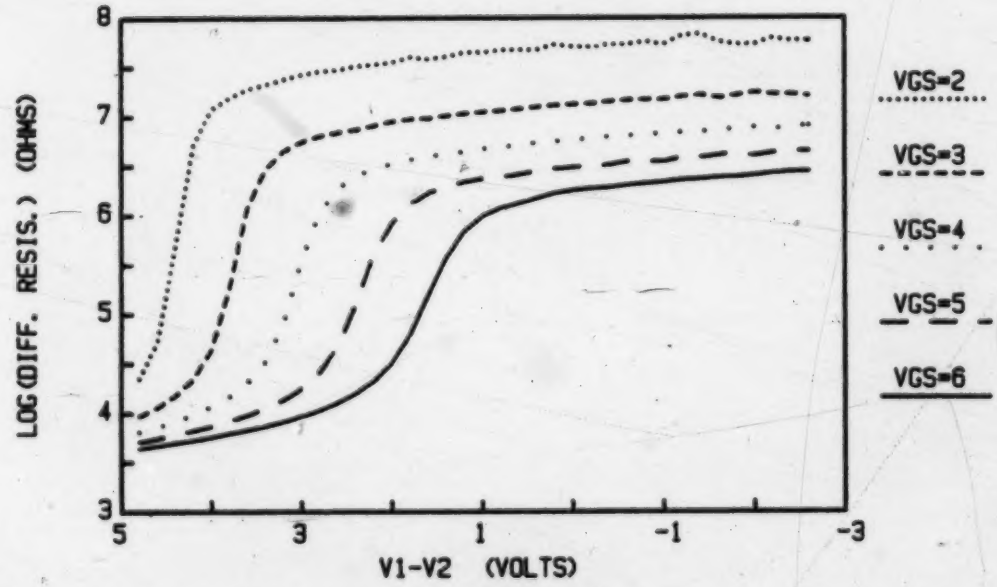

Fig. C19 As in Fig. C16, but for the long MAGFET (W/L=25μm/100μm).

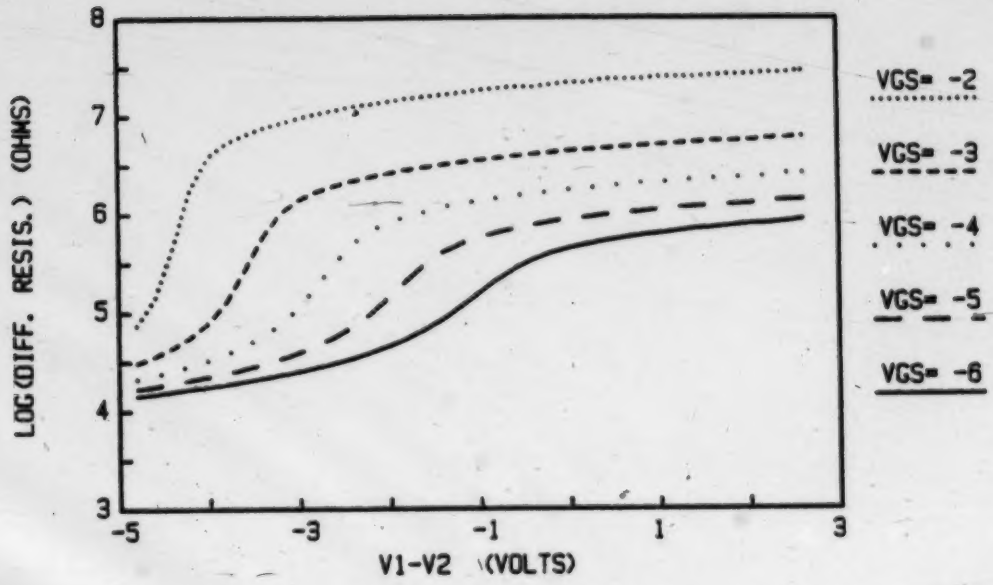

Fig. C20 As in Fig. C16, but for the PMOS MAGFET (W/L=75μm/25μm).

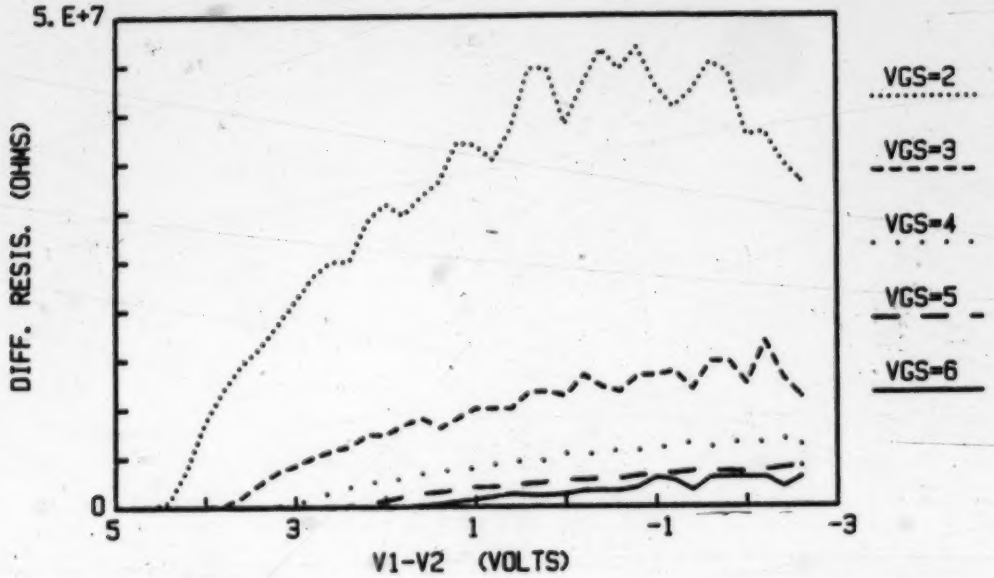

Fig. C21 Incremental resistance between drains as a function of drain voltage difference at various values of V_{GS}, of the square dual drain MAGFET (W/L=100μm/100 μm), fabricated via Northern Telecom. (V1-V2)=(V_{D1}-V_{D2}).

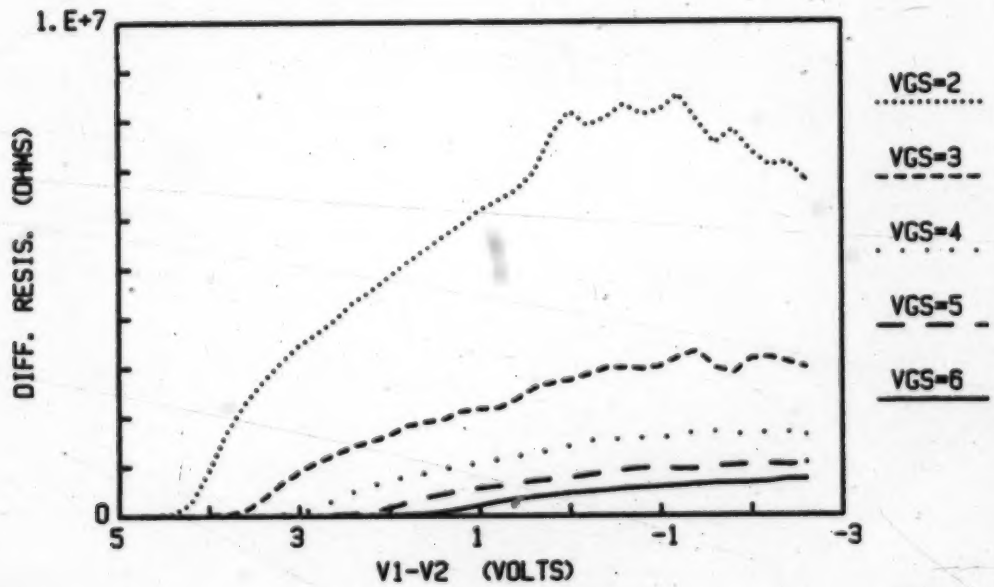

Fig. C22 As in Fig. C21, but for the square MAGFET (W/L=25μm/25μm).

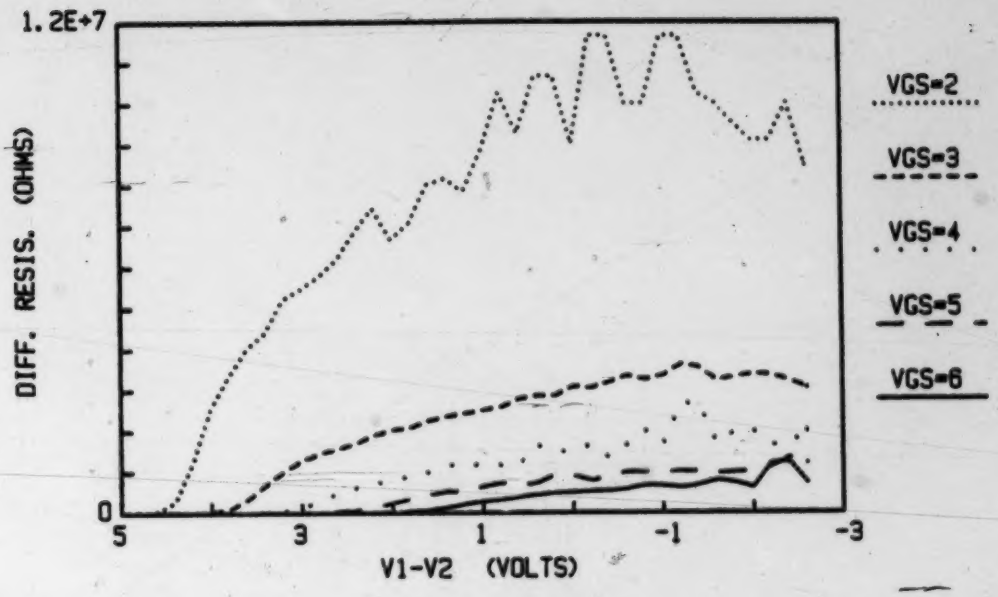

Fig. C23 As in Fig. C21, but for the wide MAGFET (W/L=100μm/25μm).

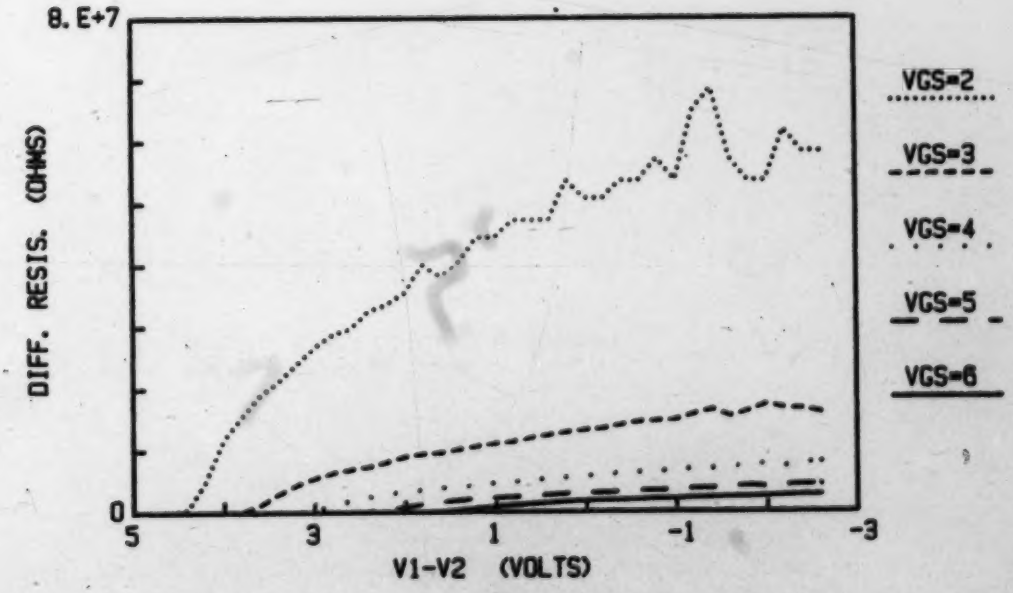

Fig. C24 As in Fig. C21, but for the long MAGFET (W/L=25μm/100μm).

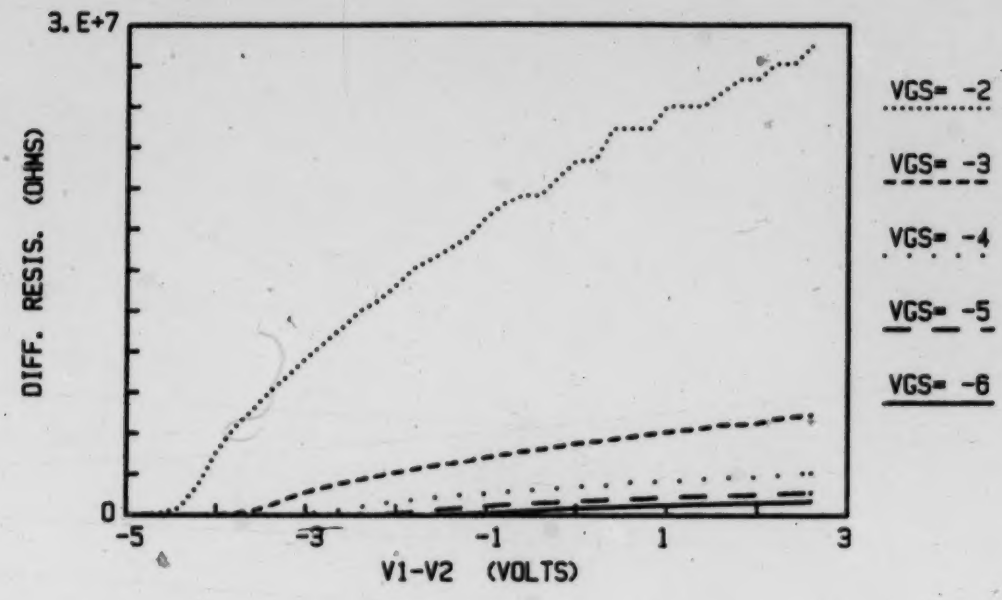

Fig. C25 As in Fig. C21, but for the PMOS MAGFET (W/L=75μm/25μm).